Design of High Performance Arithmetic and Logic Circuits in DSM Technology

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Abstract— **Dynamic domino logic circuits are widely used in modern digital VLSI circuits. These dynamic circuits are often favoured in high performance designs because of the speed advantage offered over static CMOS logic circuits. The main drawbacks of dynamic logic are a lack of design automation, a decreased tolerance to noise and increased power dissipation. However, domino gates typically consume higher dynamic switching and leakage power and display weaker noise immunity as compared to static CMOS logic circuits. In this work, a new low voltage swing circuit technique based on a dual threshold voltage CMOS technology is presented for simultaneously reducing active & standby mode power consumption and enhancing evaluation speed and noise immunity in domino logic circuits in 65 nm deep submicron technology (DSM). The proposed technique modifies both the upper and lower boundaries of the voltage swing at the dynamic node. Ground, power supply and threshold voltages are simultaneously optimized to minimize the power delay product (PDP). The proposed techniques are compared by performing detailed transistor simulations on benchmark circuits such as 1-bit Half Adder, 16-bit Adder, 16-bit Comparator, D-Latch, 4-bit LFSR using Microwind 3 and DSCH3 CMOS layout CAD tools.**

Index Terms—**CMOS, DSM technology, Domino logic, Dynamic power, Full-swing, Power, Power delay product, Reduced-swing.**

I. INTRODUCTION

The power consumed in high performance microprocessors has increased to levels that impose a fundamental limitation to increasing performance and functionality [1]–[3]. If the current trend in increasing power continues, high performance microprocessors will soon consume thousands of watts. The power density of a high performance microprocessor will exceed the power density levels encountered in typical rocket nozzles within the next decade [2]. The generation, distribution, and dissipation of power are at the forefront of current problems faced by the integrated circuit industry [1]–[5]. The application of aggressive circuit design techniques which only focus on enhancing circuit speed without considering power is no longer an acceptable approach in most high complexity digital systems.

Dynamic switching power, the dominant component of the total power consumed in current CMOS technologies, is quadratically reduced by lowering the supply voltage. Lowering the supply voltage, however, degrades circuit speed due to reduced transistor currents. Threshold voltages are scaled to reduce the degradation in speed caused by supply voltage scaling while maintaining the dynamic power consumption within acceptable levels [1]–[5]. At reduced threshold voltages, however, subthreshold leakage currents increase exponentially. Energy efficient circuit techniques aimed at lowering leakage currents are, therefore, highly desirable. Domino logic circuit techniques are extensively applied in high performance microprocessors due to the superior speed and area characteristics of domino CMOS circuits as compared to static CMOS circuits [7]–[8]. However, deep sub micrometer (DSM) domino logic circuits utilizing low power supply and threshold voltages have decreased noise margins [9]–[11]. As on-chip noise becomes more severe with technology scaling and increasing operating frequencies, error free operation of domino logic circuits has become a major challenge [9], [10], [11].

The focus of this paper is to implement various Reduced-swing domino logic circuit techniques which offer better speed, energy-efficiency and noise immunity in DSM technology. The organization of the paper is as follows. A brief review of the sources of power dissipation in CMOS circuits is provided in Section II. In Section III various reduced-swing techniques in domino logic circuits for power reduction are proposed. In Section IV simulation and implementation results are presented. Finally, conclusions are presented in Section V.

II. SOURCES OF POWER DISSIPATION

The power consumed by CMOS circuits can be classified into two categories:

A. Dynamic Power Dissipation

For a fraction of an instant during the operation of a circuit, both the PMOS and NMOS devices are "on" simultaneously. The duration of the interval depends on the input and output transition (rise and fall) times. During this time, a path exists between V_{DD} and G_{nd} and a short-circuit current flows. However, this is not the dominant factor in dynamic power dissipation. The major component of dynamic power dissipation arises from transient switching behaviour of the nodes. Signals in CMOS devices transition back and forth between the two logic levels, resulting in the charging and discharging of parasitic capacitances in the circuit. Dynamic power dissipation is proportional to the square of the supply voltage. In deep sub-micron processes, supply voltages and threshold voltages for MOS transistors are greatly reduced. This, to an extent, reduces the dynamic power dissipation.

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B. Static Power Dissipation

This is the power dissipation due to leakage currents which flow through a transistor when no transactions occur and the transistor is in a steady state. Leakage power depends on gate length and oxide thickness. It varies exponentially with threshold voltage and other parameters. Reduction of supply voltages and threshold voltages for MOS transistors, which helps to reduce dynamic power dissipation, becomes disadvantageous in this case. The subthreshold leakage current increases exponentially, thereby increasing static power dissipation.

III. CIRCUIT TECHNIQUES

Dynamic domino logic circuits are widely used in modern VLSI circuits. These dynamic circuits are often favoured in high performance designs because of the speed advantage offered over static CMOS logic. The main drawbacks of dynamic logic are a lack of design automation, a decreased tolerance to noise and increased power dissipation. This work discusses several dual threshold voltage domino circuit design techniques to reduce the power dissipation of domino logic while simultaneously improving noise immunity. The benefits are achieved by limiting the voltage swing of the internal dynamic node in a typical domino gate. This dynamic storage node is the node connected to the input of the output inverter of a domino gate as shown in fig.1.
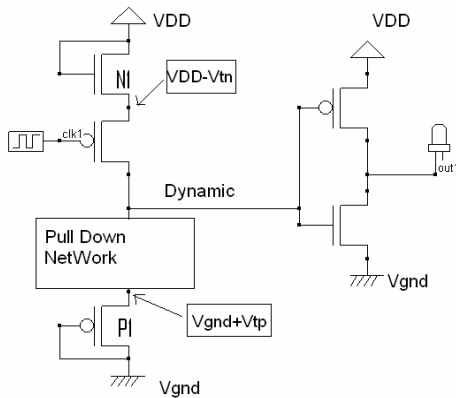

Fig.1. Dynamic node low voltage swing domino logic circuit

The above circuit is used to reduce the voltage swing at the dynamic node of a domino gate. N1, P1 remains always ON, therefore dynamic node voltage swing is from $V_{gnd}+V_{tp}$ to $V_{DD}-V_{tn}$. This technique can reduce the energy required to charge /discharge the dynamic node of a domino gate. In the precharge phase, clock is low, dynamic node is charged to $V_{DD}-V_{tn}$ by precharge transistor, output node is discharged to V_{gnd} by N2. In evaluation phase, clock is high, the voltage at the dynamic node depends on pull-down network. In this circuit PMOS and NMOS transistors within the output inverter are simultaneously turned ON, producing a significant short-circuit current during both active mode and idle modes of operation. Short circuit

current produced by the output inverter diminishes the active mode power savings and increases the idle mode power consumption. Propagation delay is also increased due to the significantly degraded gate overdrive of both transistors in the output inverter. A complete analysis of the effects of the reduced swing at the dynamic node on both noise tolerance and propagation delay is presented with respect to specific circuit configurations below.

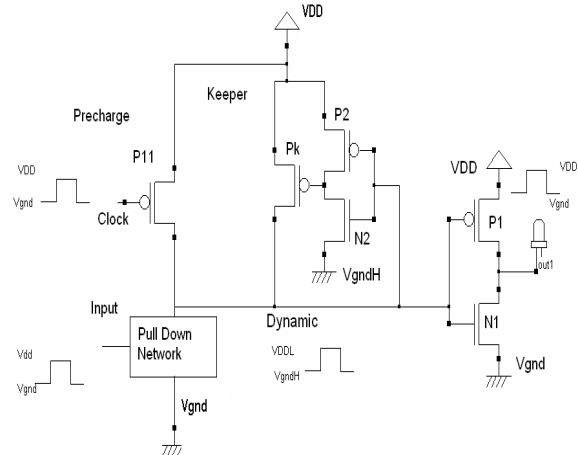*A. Single V_t domino logic circuit with keeper:*

Fig.2. Domino logic circuit with keeper.

The single V_t domino logic circuit with keeper is shown in Fig.2. In the precharge phase, clock is low, dynamic node is charged to V_{DD} by precharge transistor, output node is discharged to V_{gnd} by N1. The evaluation phase begins when the clock transitions high, dynamic node is discharged to V_{gnd} through pull down network provided that the inputs are high, output node is charged to V_{DD} by P1. If any of the inputs are low, the voltage at the dynamic node depends on the pull-down network. Keeper circuit is used to maintain the voltage level at dynamic node which also increases the noise immunity. The voltage at the dynamic node should be V_{DD} but gets diminished due to several reasons, by using the keeper in the above circuit with P2, N2 transistors pair forming inverter turns ON Pk transistor which pulls dynamic node to V_{DD}.

B. Single V_t domino logic circuit with dual power supply, dual ground:
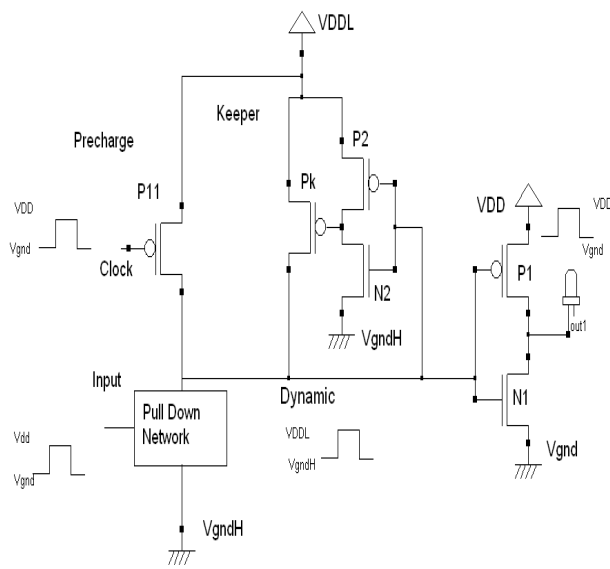

Fig.3. The dynamic node low voltage swing domino circuit technique with dual power supplies and ground voltages $V_{DDL} < V_{DD}$, $V_{gndH} > V_{gnd}$

The single V_t domino logic circuit with dual power supply, dual ground is shown in Fig.3. In the precharge phase, clock is low, the dynamic node is charged to V_{DDL} by precharge transistor, output node is discharged to V_{gnd} by N1, P1 is weakly inverted. Weak inversion current produced by P1 depends on the upper boundary of voltage swing (V_{DDL}) at the dynamic node and threshold voltage of P1 (V_{tp1}). Evaluation phase begins when the clock transitions high. Dynamic node is discharged to V_{gndH} through pull down network provided that the inputs are high. Output node is charged to V_{DD} by P1, N1 is weakly inverted .Weak inversion current conducted by N1 depends on the lower boundary of voltage swing (V_{gndH}) at the dynamic node and threshold voltage of N1 (V_{tn1}). The voltage swing at the dynamic node is from V_{gndH} to V_{DDL} while the voltages at the output, clock and input nodes are maintained full swing between V_{gnd} and V_{DD} for high speed operations. V_{DDL} and V_{gndH} are chosen as optimized values to minimize the power consumption

C. Dual Vt Domino Logic circuit With Dual power supply, Dual Ground(N1 High Threshold):

The dual V_t domino logic circuit with dual power supply, dual ground (N1 high threshold) is shown in Fig.4. The NMOS transistor in the output inverter has high V_t. Short circuit current is therefore reduced only in the evaluation phase if the inputs are high. Hence evaluation speed of the circuit is higher as compared to N1, P1 high threshold technique.
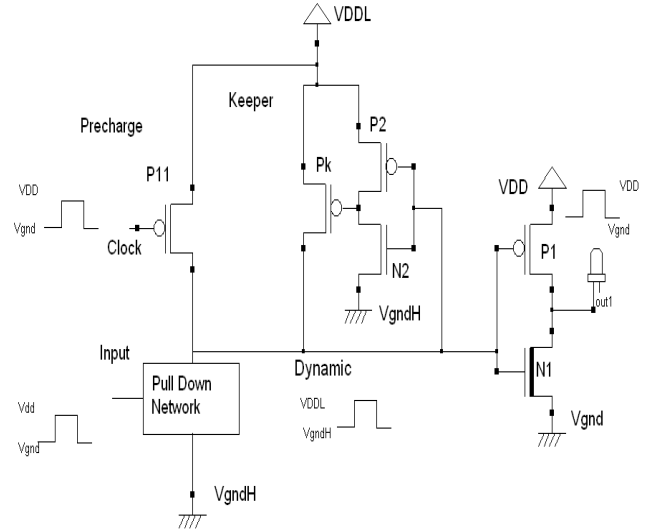

Fig.4. The dynamic node low voltage swing domino circuit technique with dual power supplies and ground voltages $V_{DDL} < V_{DD}$, $V_{gndH} > V_{gnd}$ and with N1 high threshold

D. Dual V_t domino logic circuit with dual power supply, dual ground (N2 ground):
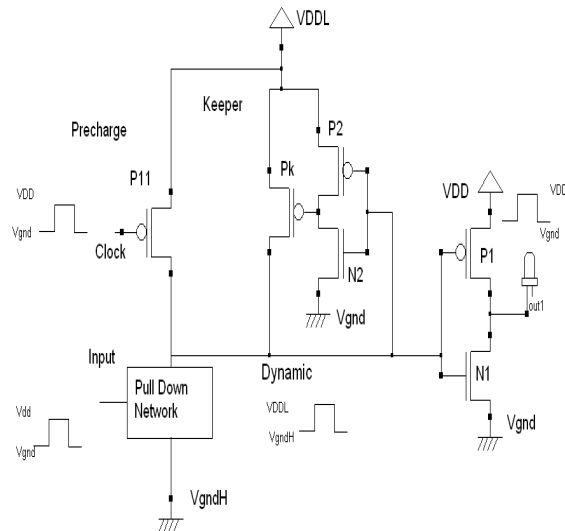

Fig.5. The dynamic node low voltage swing domino circuit technique with dual power supplies and ground voltages $V_{DDL} < V_{DD}$, $V_{gndH} > V_{gnd}$ and with N2 Ground

The dual V_t domino logic circuit with dual power supply, dual ground (N1 high threshold) is shown in Fig.5. N2 FET is grounded; these modifications are made to the basic circuit in

order to analyze the variations in the parameters like power, delay, area, power delay product (PDP) and to find the efficient technique.

E. Dual V_t domino logic circuit with dual power supply, dual ground (N1, P1 high threshold):
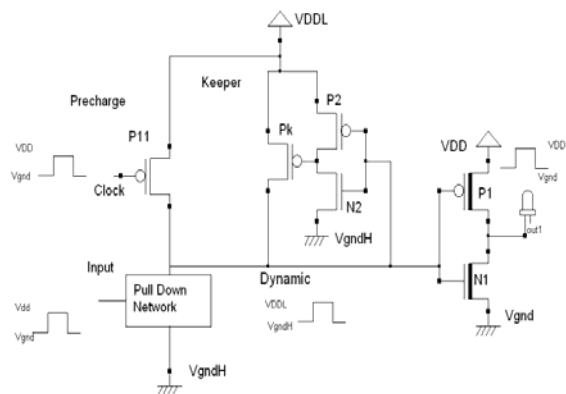

Fig.6. The dynamic node low voltage swing domino circuit technique with dual power supplies and ground voltages $V_{DDL}<V_{DD}$, $V_{gndH}>V_{gnd}$ and with N1, P1 high thresholds

The dual V_t domino logic circuit with dual power supply, dual ground (N1, P1 High Threshold) is shown in Fig.6. The short circuit current produced by the output inverter is suppressed during both the precharge and evaluation phases of operation, since the NMOS and PMOS transistors in the output inverter have high V_t. However, evaluation speed is also degraded due to the weaker pull-up strength of high V_t PMOS transistor.

F. Dual V_t domino logic circuit with dual power supply,

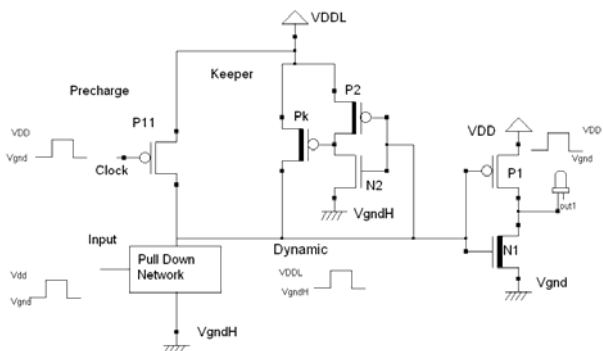*dual ground (Pk, P2, N1 high threshold):*

Fig.7. The dynamic node low voltage swing domino circuit technique with dual power supplies and ground voltages $V_{DDL}<V_{DD}$, $V_{gndH}>V_{gnd}$ and with N1, P2, Pk high thresholds

The dual V_t domino logic circuit with dual power supply, dual ground (Pk, P2, N1 high threshold) is shown in Fig.7.

Pk, P2, N1 FETs threshold voltages are increased, these modifications are made to the basic circuit in order to analyze the variations in the parameters like power, delay, area, power delay product (PDP) and to find the efficient technique.

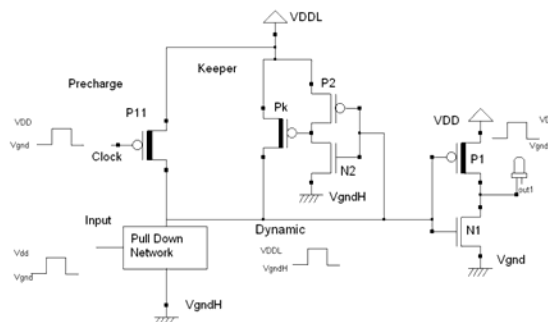*G. Dual V_t domino logic circuit with dual power supply, dual ground (P11,PK,P1 high threshold):*

Fig.8. The dynamic node low voltage swing domino circuit technique with dual power supplies and ground voltages $V_{DDL}<V_{DD}$, $V_{gndH}>V_{gnd}$ and with Pk, P1, P11 High thresholds

The dual V_t domino logic circuit with dual power supply, dual ground (P11, PK, P1 High threshold) P11, Pk, P2 FETs threshold voltages are increased, these modifications are made to the basic circuit in order to analyze the variations in the parameters like power, delay, area, power delay product (PDP) and to find the efficient technique.

IV. SIMULATION AND IMPLEMENTATION RESULTS

In this work, the benchmark circuits using the stated seven techniques are implemented. The figures of merits used to compare these techniques are power consumption, propagation delay and power delay product (PDP). The benchmark circuits implemented are 1-bit Half Adder, 16-bit Adder, 16-bit Comparator, D-Latch, 4-bit LFSR. These design styles are compared by performing detailed transistor-level simulations on benchmark circuits using DSCH3 and Microwind3 CAD tool in 65 nm technology. The results of the benchmark circuits for all techniques are given below. Table1 shows the comparison of all the seven proposed techniques for 1-bit Half Adder. Table2 shows the comparison of all the techniques for 16-bit Adder. Table3 shows the comparison of all the techniques for 16-bit Comparator. Table4 shows the comparison of all the techniques for D-Latch. Table5 shows the comparison of all the techniques for 4-bit LFSR. From the results, it can be observed that the proposed logic techniques provide lower values of power dissipation, propagation delay and PDP when compared to the standard domino logic structure.

Table 1. Optimum Values for 1-bit Half Adder:

TECHNIQUES	POWER(µw)	DELAY(ns)	PDP(10^{-15} w-s)	Area(micro sq.meter)
Domino with Keeper	92.33	0.053	4.6116	114.5644
N2 GROUND	60.025	0.064	3.8415	126.742
Dual Supply	60.158	0.064	3.85	136.269
PK, P11, P1 High threshold	71.981	0.064	4.606	136.21
PK, P2, N1 High threshold	67.982	0.051	3.467	136.041
P1, N1 High threshold	68.77	0.064	4.4012	137.182
N1 High threshold	67.99	0.064	4.3519	154.249

Table 2. Optimum Values for 16-bit Adder:

S.NO	TECHNIQUES	POWER(mw)	DELAY(ns)	PDP(10^{-12} w-s)	Area(micro sq.meter)
1	Domino with Keeper	11.062	0.024	0.2654	12809.5
2	N2 GROUND	10.958	0.022	0.241	12826.9
3	Dual Supply	11.402	0.021	0.2394	13782
4	PK, P11, P1 High threshold	12.088	0.021	0.2538	12159.48
5	PK, P2, N1 High threshold	20.15	0.022	0.4433	15409.67
6	P1, N1 High threshold	21.88	0.022	0.4813	15269
7	N1 High threshold	10.245	0.047	0.4815	10371

Table 3. Optimum Values for 16-bit Comparator:

S.NO	TECHNIQUES	POWER	DELAY	PDP(10^{-15} w-s)	Area(micro sq.meter
1	Domino with Keeper	10.475µW	0.064nS	0.6704	18914
2	N2 GROUND	8.204µW	0.059nS	0.484	19316
3	Dual Supply	7.795µW	0.064nS	0.4988	18329.6
4	PK, P11, P1 High threshold	8.457µW	0.064nS	0.5412	18369.4
5	PK, P2, N1 High threshold	8.506µW	0.065nS	0.5528	20240.6
6	P1, N1 High threshold	10.432µW	0.064nS	0.6676	18453
7	N1 High threshold	8.560µW	0.063nS	0.5392	18840

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Table4. Optimum Values for D-Latch:

S.NO	TECHNIQUES	POWER(mw)	DELAY(ns)	PDP(10^{-12} w-s)	Area(micro sq.meter)
1	Domino with Keeper	0.158	0.056	8.848	215.56
2	N2 GROUND	0.163	0.075	12.22	254.92
3	Dual Supply	0.22	0.058	12.76	261.41
4	PK, P11, P1 High threshold	0.169	0.078	13.18	258.69
5	PK, P2, N1 High threshold	0.169	0.058	9.8	262.885
6	P1, N1 High threshold	0.169	0.078	13.18	256.11
7	N1 High threshold	0.169	0.078	13.18	262.59

Table5. Optimum Values for 4-bit LFSR:

TECHNIQUES	POWER(mw)	DELAY(ns)	PDP(10^{-12} w-s)	Area(micro sq.meter)
Domino with Keeper	4.587	0.049	0.2247	2255.05
N2 GROUND	2.976	0.056	0.1666	2493.05
Dual Supply	2.882	0.065	0.1873	2472.36
PK, P11, P1 High threshold	3.08	0.065	0.2002	2468.4
PK, P2, N1 High threshold	2.929	0.065	0.1903	2482.7
P1, N1 High threshold	2.889	0.065	0.1877	2463.3
N1 High threshold	2.968	0.065	0.1929	2483.34

V.CONCLUSIONS

In the deep submicron technology, power delay product must be reduced to increase the efficiency of a circuit. The circuit techniques employing dual thresholds, dual voltages, dual grounds are presented in this work for simultaneously reducing power dissipation and delay in domino circuits and also to increase the noise immunity. The parameters of power dissipation, delay and power delay product are calculated for 1-bit Half Adder, 16-bit Adder, 16-bit Comparator, D-Latch, 4-bit LFSR using different techniques in 65nm technology. From the results it can be concluded that the proposed logic technique which is dual threshold, dual ground and dual supply voltage with N1 high threshold shows good performance when compared to single threshold domino logic techniques. Hence it can be concluded that CMOS logic techniques proposed in this work yield low power, high performance operation with increased noise immunity. Hence, it is concluded that the proposed designs will provide a platform for designing high performance and low power digital circuits such as processors and multipliers.

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