A Single Op Amp Digitally Programmable Circuit for Minimal Realization of Arbitrary Gains

T S Rathore

Dean R&D, Head ET Department
St Francis Institute of Technology, Mumbai 400 103, India

Abstract— **Three different configurations have been reported for programming explicitly inverting, positive fractional and non-inverting gains, respectively. This paper proposes a single operational amplifier digitally programmable circuit for a set of arbitrary gains, which may include inverting, positive fractional and/or non-inverting gains, with minimum number of elements. The design procedure is illustrated with an example.**

Keyword- Amplifier, Programmable amplifier, Digitally programmable amplifier

I. INTRODUCTION

Three different configurations for realizing explicitly negative, positive fractional and positive gains are shown in Fig. 1 (a), (b) and (c), respectively [1].
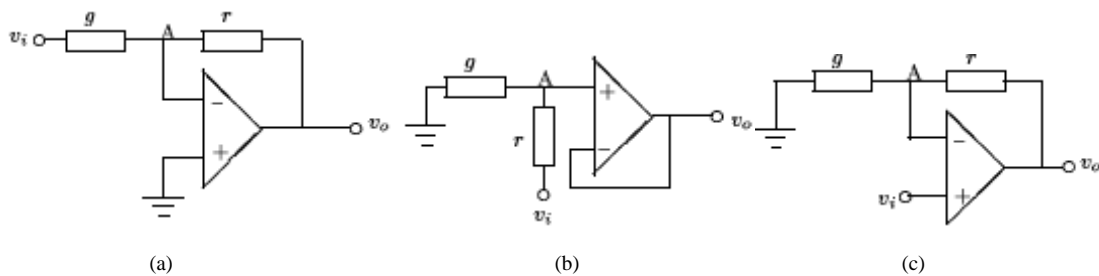

Fig. 1. (a) Inverting amplifier, (b) Buffered Attenuator, (c) Non-inverting amplifier

It is possible to derive a general amplifier for an arbitrary gain by using switches. Close examination of Fig. 1 revels that each configuration uses 1 OA and two resistors connected suitably. It should, therefore, be possible that any one of the amplifier circuits can be converted into the other two by disconnecting some connections and reconnecting them suitably. For example, inverting amplifier circuit of Fig. 1(a) can be converted into that shown in (b) by the following procedure.

1. Disconnect g from v_i and reconnect to ground.
2. Disconnect r from v_o and reconnect to v_i.
3. Disconnect non-inverting terminal (+) of the operational amplifier from earth and reconnect to node A.
4. Disconnect inverting terminal (-) terminal of the operational amplifier from node A and reconnect to v_o.
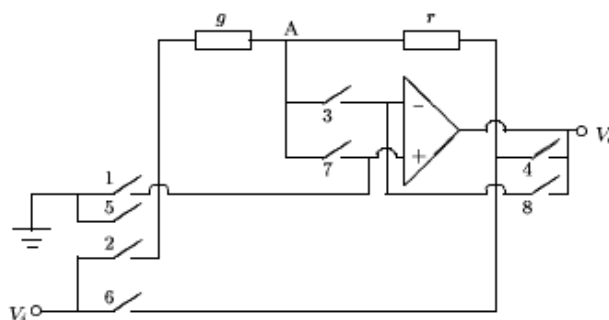

Fig. 2. A general amplifier for realizing an inverting gain and/or a positive attenuation

Obviously, minimum 8 switches would be required to carry out the above operations as shown in Fig. 2: switches 1-4 to be closed (opened) and switches 5-8 to be opened (closed) for realizing an inverting (positive fractional) gain.

Similarly, one can easily verify that the amplifier in Fig. 1(a) can be converted into that shown in (c) by providing minimum 4 additional switches: two switches for disconnecting g from v_i and reconnecting it to ground and two for disconnecting + terminal from ground and reconnecting it to v_i.

Further, one can verify that the circuit of Figure 1(a) can be converted into both (b) and (c) by providing minimum 9 additional switches as shown in Fig. 3. Switches 1-8 are required for converting an inverting amplifier into a positive attenuator and vice versa and one additional switch 9 is required to convert the inverting amplifier into the non-inverting amplifier and vice versa.
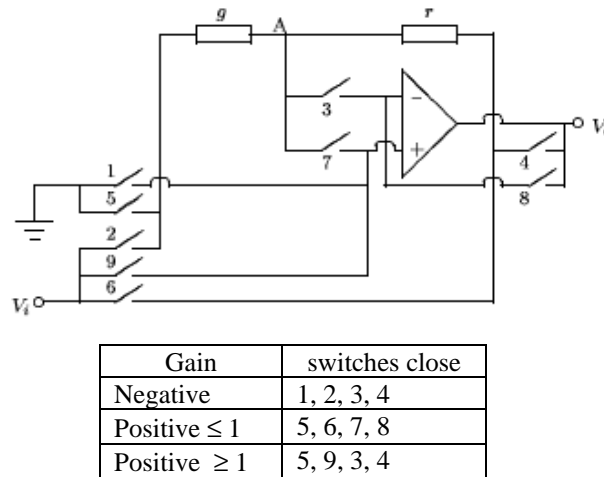

Gain	switches close
Negative	1, 2, 3, 4
Positive ≤ 1	5, 6, 7, 8
Positive ≥ 1	5, 9, 3, 4

Fig. 3. A general amplifier for realizing an arbitrary gain value

II. GENERAL PROGRAMMABLE GAIN AMPLIFIER

A set of N gains consisting of N_{AI} inverting, N_{AA} positive fractional and N_{AN} non-inverting gains can be programmed as follows.

(i)   Convert all the gains into gains of any one type, say inverting one, using the following relations.

$$|A_I| = 1/A_A \quad 1, \qquad |A_I| = A_N \quad 1 \qquad (1)$$

Let η be the number of total finite non-zero inverting gains after this conversion.

(ii)   Realize η inverting gains by a programmable inverting amplifier with the minimum number of elements (resistors, Op Amp and switches) following the methods given in [1][2].

(iii)   Realize the other gains with the additional switches as shown in Fig. 3.

The number of additional switches required is determined from the table given in Fig. 3 as follows.

1. Note that the switches 1, 2, 6, 7, 8 and 9 operate only for one particular type of gains: 1 and 2 for inverting, 6, 7 and 8 for positive fractions and 9 for non-inverting. The switches 3 and 4 operate for both inverting and non-inverting types of gains, and the switch 5 operate for both positive fractional and non-inverting gains. We shall call the switches 1-2, 6-9 as single gain type and 3, 4 and 5 as dual gain type switches.

2. Switches 1 and 2 are to be connected explicitly for any one inverting gain. Hence, 2 sets of N_{AI} switches all in parallel will be required, one switch for each gain in N_{AI}

3. Similarly, switches 6, 7, 8 are explicitly required for realizing any one attenuation. Hence, 3 sets of N_{AN} parallel switches will be required, one switch for each gain in N_{AA}.

4. An additional switch 9 is required for realizing any one non-inverting gain. Hence, N_{AN} switches in parallel will be required, one switch for each gain in N_{AN}.

5. Switch 5 is required for realizing one positive attenuation and one non-inverting gain. Hence, one set of $N_{AA} + N_{AN}$ switches will be required, one for each gain in N_{AA} and N_{AN}.

6. Similarly, switches 3 and 4 are required for realizing one inverting and one non-inverting gain. Hence, 2 sets of $N_{AI} + N_{AN}$ parallel switches will be required, one switch for each gain in N_{AI} and N_{AN}. Thus, the number of additional switches required is

$$(2N_{AI} + 3N_{AA} + N_{AN}) + (N_{AA} + N_{AN}) + 2(N_{AI} + N_{AN}) = 4N_{AI} + 4N_{AA} + 4N_{AN} = 4N \tag{2}$$

The number of total switches required is

$$N_S = N + 4N = 5N. \tag{3}$$

7. If the number of switches in a bank equals the number of specified gains, then they all can be replaced by a short.

Based on the above theory, we state the following theorem.

A minimal realization of a set of N arbitrary programmable gains requires 1 OA, η + 1 resistors and N + N_S switches where η is the total number of actual finite non-zero inverting gains realized.

It is interesting to note that Genin's theorem [3] is a special case of this theorem for only positive gains with the lowest gain value as 1.

III. DESIGN

The design procedure for the general programmable amplifier of Fig. 3 is formulated as follows.

1. Convert each gain A_A and A_N into A_I as per eqn (1).

2. Arrange all the converted inverting gains in an ascending order.

3. Determine the resistor values using the design relations for realizing these inverting gains as an inverting type PGA [1][2].

4. Replace each of the switches 1-9 by a bank of parallel switches as follows. Replace all the single gain type switches 1, 2 by N_{AI} parallel switches, 6, 7, 8 by N_{AA} parallel switches, 9 by N_{AN} parallel switches. Replace the dual gain type switches 3, 4 by $N_{AA} + N_{AN}$ parallel switches, 5 by $N_{AA} + N_{AN}$ parallel switches.

5. If in a particular bank of switches, the number of switches equal to the total number of specified gains, then all these switches can be replaced by one short.

A. Example

Design a minimal programmable gain amplifier for the gains -7, -2, -1, 1/4, 1/2, 1, 3. Determine the numbers of resistors and switches required. What would be these numbers if the attenuations ¼ and 1/2 are not required and when non-inverting gains 1 and 3 are also not required?

Using eqn (1), the following conversion table is obtained.

TABLE I. CONVERSION TABLE

Specified gain A_N $\rightarrow$	-7	-2	-1	1/4	1/2	1	3
Converted gain $|A_I|$ $\rightarrow$	7	2	1	3	1	0	2

Hence, the gains to be programmed, arranged in ascending order, are $|A_I| \rightarrow$ 0, 1, 2, 3, 7. The finite non-zero inverting gains are 1, 2, 3, 7. Thus, $\eta = 4$.

One minimal programmable inverting amplifier is obtained as an S-ladder realization from [1][2]. Then the complete programmable gain amplifier for the specified gains is obtained as shown in Fig. 4 in which the switches 1-9 are replaced by banks of parallel switches.

The number of resistors $N_R = \eta + 1 = 5$. The number of switches required, from eqn (3), is $N_S = N + 4N = 35$. If the two attenuations 1/4 and 1/2 are not to be programmed, then η (the finite non-zero inverting gains 1, 2, 7) will become 3. Hence, $N_R = 4$ and the number of switches $= 5 + 4N_{AI} + 4N_{NI} = 5 + 4\times 3 + 4 \times 2 = 25$.

The eight switches corresponding to the attenuations of ¼ and 1/2 in the switch banks 5, 6, 7 and 8 in Fig. 4 will appear as open circuits and, therefore, can be eliminated. Finally, the switch banks 3 and 4 have the number of switches equal to the number of gains to be programmed; they can be replaced by shorts.
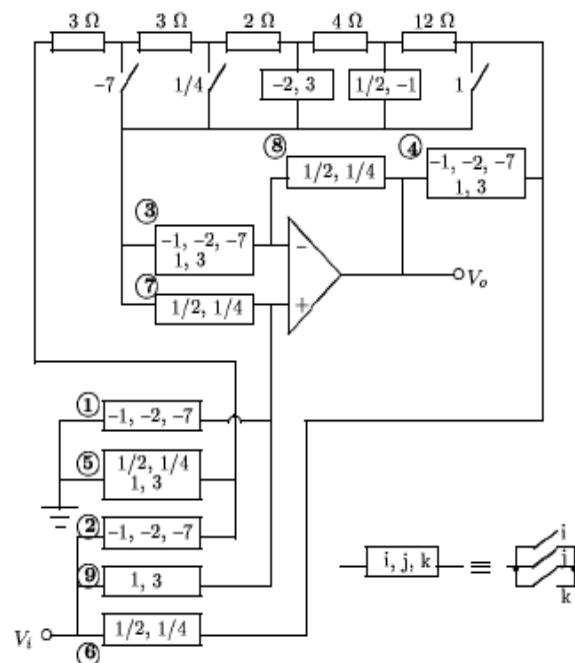

Fig. 4. Amplifier for the Example

If the gains 1 and 3 are also not to be programmed, then η remains as 3. Hence, $N_R = 4$. Now the switches corresponding to the gains 1 and 3 in the switch banks 3, 4, 5, 9 will be opened. Note that the number of parallel switches in each of the switch banks 1, 2, 3 and 4 equals the number of the specified gains. Hence, these switches can be replaced by shorts. Thus, the total number of switches required will be only 3.

IV. CONCLUSION

A general circuit configuration capable of programming a set of N arbitrary gains with one OA, $4N$ switches and $\eta + 1$ resistors has been proposed. The design procedure has been illustrated with an example.

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AUTHORS PROFILE

T S Rathore was born in Jhabhua (M P, India) on Oct. 29, 1943. He received the B Sc (Electrical Engineering), M E (Applied Electronics & Servomechanisms), and Ph D (by research on Passive and Active Circuits) degrees in electrical engineering from Indore University, Indore, India in 1965, 1970 and 1975, respectively.

He served SGSITS, Indore from 1965 to 1978 before joining the EE Department of IIT Bombay from where he retired as a Professor on superannuation in June 2006. Currently, from July 2006, he is the Dean (R&D) and Head of Electronics & Telecommunication Department at St. Francis Institute of Technology, Borivali.

He was a post-doctoral fellow (1983-85) at the Concordia University, Montreal, Canada and a visiting researcher at the University of South Australia, Adelaide (March-June 1993). He was an ISTE visiting professor (2005-2007). He has published and presented over 200 research papers in various national/international journals and conferences. He has authored the book Digital Measurement Techniques, New Delhi: Narosa Publishing House, 1996 and Alpha Science International Pvt. Ltd., U K, 2003 and translated in Russian language in 2004. He was the guest editor of the special issue of Journal of IE in Instrumentation Electronics (1992). He is a member on the editoral boards of ISTE National Journal of Technical Education and IETE Journal of Education. He has witnessed, organized and chaired many national/international conferences and in some he was also the chief editor of the proceedings.

His areas of teaching and research interest are Analysis and Synthesis of Networks, Electronic Circuit Design, Switched-Capacitor Filters, Electronic-Aided Instrumentation, Hartley Transform, Signal Processing, Fault Diagnosis and Knowledge-Based Systems.

Prof. Rathore is a Senior Member of IEEE (USA), Fellow of IETE (India), Fellow of IE (India), Member of ISTE (India), Member of Instrument Society of India, Member of Computer Society of India. He has been listed in Asia's Who's Who of Men and Women of achievement (1991). He has played a very active role as Fellow of IETE and has served its Mumbai Centre as Volunteer member (1997-98), Co-opted member (1998-99), Secretary (1999-2000), Chairman (2001-02), Vice Chairman (2003-06) and Chairman (2006-08).

He has received IETE M N Saha Memorial Award (1995), IEEE Silver Jubilee Medal (2001), ISTE U P Government National Award (2002), ISTE Maharashtra State National Award (2003), ISTE Prof S V C Aiya Memorial Award (2004), IETE BR Batra Memorial Award (2005), IETE Prof K Sreenivasan Memorial Award (2005). IETE K S Krishnan Memorial Award (2009) and IETE - Hari Ramji Toshniwal Gold Medal (2010).