Power Efficient Probabilistic Multiplier for Digital Image Processing Subsystems

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***Abstract*—Power efficient is an important availability for various image processing subsystems and portable devices applications. The design of proposed probabilistic multiplier is to trade a lesser amount of accuracy with reduced power consumption. In this paper, the probabilistic multiplier is eliminating the some part of the partial product generating path in least significant bit to reduce the power consumption and transistor count. The power consumption and probabilistic error behaviour of the proposed multiplier is verified and compared with other multipliers.**

Keyword-Acceptable Accuracy, Partial Product Generation Path, Probabilistic Approach, Minimum Absolute Mean Error, Image processing Subsystem

I. INTRODUCTION

Multipliers are the basic blocks in different digital image processing applications such as image compression, image filtering and so on. In most of the image processing applications; human being can obtained valuable information from a little incorrect yield. The design of multiplier having low power consumption and low propagation delay results of great interest for the implementation of modern digital systems. The optimization of multipliers in terms of power, delay and transistor count have been presented in the literature [1], [2]. Braun multiplier consists of group of AND gates and adders [3]. It does not require any logic registers. This multiplier is inefficient for larger input bit widths. The Braun multiplier has produced more switching problem due to carry ripple adder in final stage.

The design of Baugh Woolley multiplier is based on carry save logic [4]. The power consumption of this multiplier depends on the number of bit sizes and the layout. It requires larger transistor counts. The booth multiplier accepts the bits in 2's complement logic based on radix-2 calculation [5], [6]. It reduces the partial product generation of the multiplier. The booth multiplier is suitable for larger input bit pattern. The design complexity of booth multiplier is due to the storage capability of secondary circuits for signed operands. Wallace tree multiplier is to minimize the partial product by the use of carry save adder trees [7]. This tree multiplier is efficient for the input bit widths of less than 32 bits. It has complex inter connection path in the layout design. The design time of this tree multiplier is very large and it consumes a lot of area.

Many research efforts have been reviewed for designing power efficient multiplier [8], [9]. The truncated multipliers are not producing all the LSB part of the partial product with reduced area and delay. It has more error for larger input bit width multiplication process. The truncation error produced from the fixed width truncated multiplier is to reduce in booth and array multiplier. Post truncated booth multiplier has lesser amount of truncation error, but it consumes larger area [10]. The process gain of these multipliers is adjusted by the different hardware logic elements.

The idea of an error tolerance and the PCMOS (Probabilistic CMOS) are important in digital image processing subsystems [11], [18] - [20]. The circuit is error tolerant if it contains faults that may cause both internal and external errors. The ways of improving chip yield by using imperfect chips in application where degradation of output quality is acceptable. The generation of acceptable results is more important than totally accurate results in digital application [12]. The n-bit ETM (Error Tolerant Multiplier) is splitting into two blocks. This multiplier contains an equal bit of two separate parts such as accurate and inaccurate multiplier part. The chance of receiving an exact product becomes possible with longer delay path [13]. The design complexity is high for these multipliers with reasonable power consumption and accuracy. The upper part of LSB values are suffered by accuracy problem for smaller as well as larger input bit width.

The approximate multipliers [14], [15] are designed by using the speculative adders to calculate the final addition of partial products. It is to reduce the critical path of summing the partial products. The LSB parts in the partial products are neglected by the use of error compensation techniques for high speed operation. The design complexity of this multiplier is high for larger input bit pattern. The imprecise multiplier architecture is

used as the basic block in a larger multiplier for high speed partial product generation. This multiplier design has an additional pre-processing unit. The extra error compensation block is used for reducing the delay [16], [17].

The implementation of probabilistic multiplier is based on probabilistic approach for modelling the behaviour of nano-metric design as well as reducing power consumption. The proposed method is to simplify the hardness of a traditional multiplier by suppressing the partial product generation path in LSB part of the multiplier. The design of an image processing subsystems using this proposed multiplier blocks and estimates this multiplier blocks in terms of accuracy and power. Any system that is not needed to estimate the accurate LSB part of the product, the proposed probabilistic multiplier has attained power, speed and transistor count by modifying the gate level implementation of LSB part of the multiplier.

II. PROPOSED PROBABILISTIC MULTIPLIER

The proposed probabilistic multiplier can split the n-bit multiplication process into two parts such as perfect part and imperfect part. The probabilistic multiplier consists of two blocks such as MSB part and LSB part. The conventional multiplier is used for the MSB part of the probabilistic multiplier to achieve high speed and high precision. The LSB part is the most essential section in the proposed multiplier as it determines the power consumption, accuracy and speed of the multiplier.

A. Power efficient LSB Part of the multiplier

The LSB part of the multiplier is divided into LSB upper part (m=n) and LSB lower part (l=n/2) for partial product free multiplication process. LSB lower part is made up of bitwise OR gates, and each of which is used to generate the result of product bit (P_0-$P_{2n/2-2}$)). The LSB upper part contains an additional AND-OR gate, which is used to produce a product output ($P_{2n/2-1}$) for upper part of the LSB and the compensation output (C_{comp}) for MSB part of the perfect multiplier. The compensator output generated from upper part LSB to MSB of the multiplier to reduce its inaccuracy. The gate level implementation of MSB part and LSB part of the proposed multiplier is shown in Fig.1.

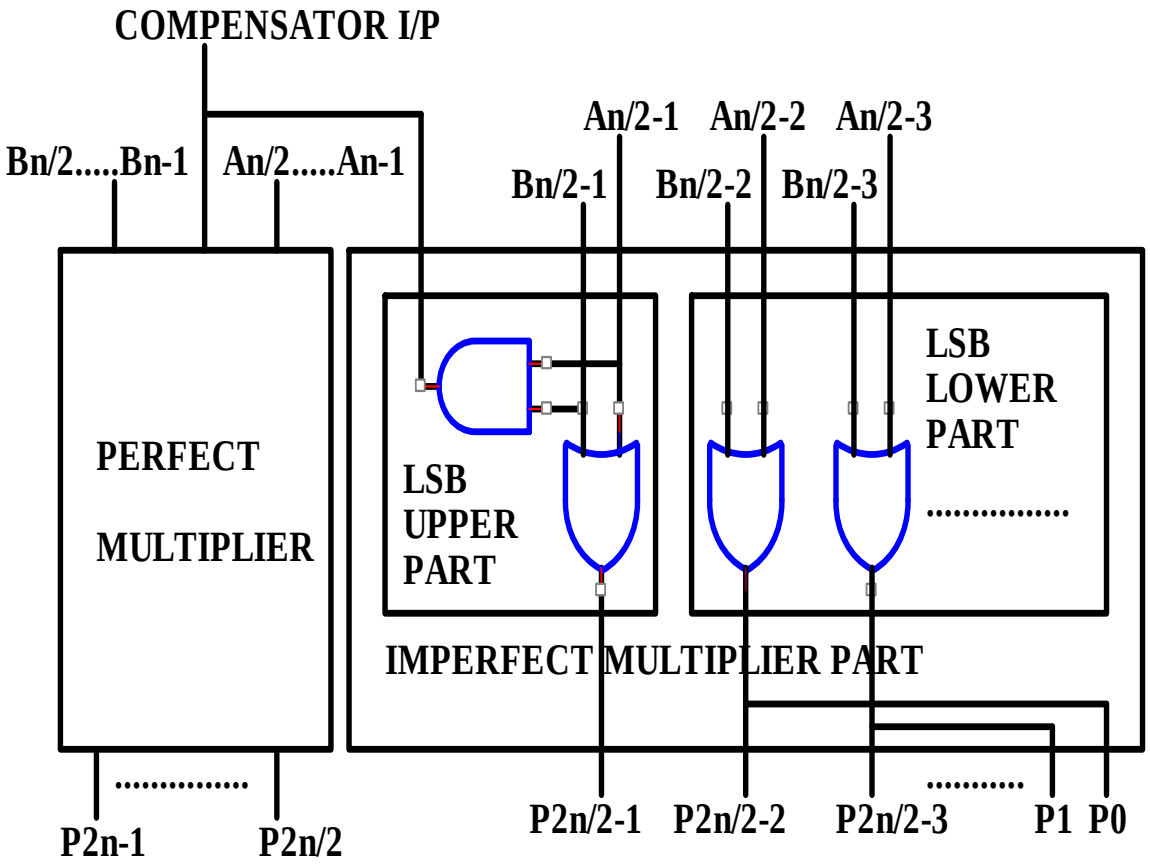

Fig.1. Gate level implementation of the proposed multiplier

B. High speed MSB Part of the Multiplier

The MSB part of the perfect multiplier is constructed by using a modified booth multiplier. The MSB part of the multiplier block is shown in Fig.2. The two inputs of perfect multipliers are the multiplicand number of A (n/2: n-1) and the multiplier number of B (n/2: n-1). The booth encoder is used to encode the multiplier [B (n/2:

n-1)] input and it produces different encoding signals. The booth decoder produces different partial products using both encoded signal from booth encoder and the multiplicand input of [A (n/2: n-1)].

The partial products produced from booth decoder are added by CSA tree (carry save adder tree) until the final two rows of partial product are remained. These final two rows are added to obtain the final product P (2n/2: 2n-1) result using CLA (carry look ahead adder). The overall delay is determined by the MSB part and also MSB part needs a fast adder. Any type of traditional multipliers can be used for this perfect multiplier part which depends on different application.

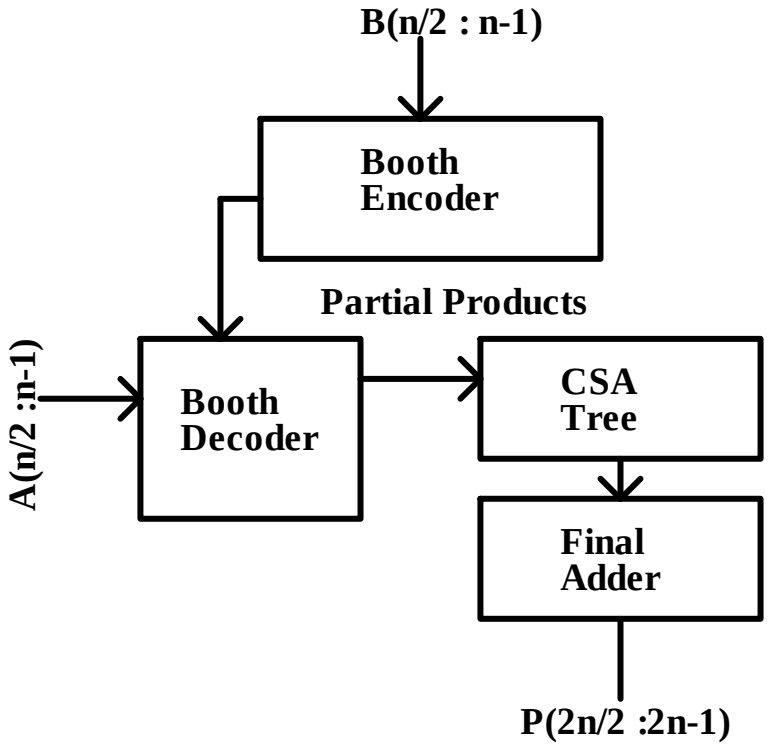

Fig.2. Block diagram for MSB part of a multiplier

C. Power Consumption of the Proposed Multiplier

The power consumption of an n-bit probabilistic multiplier depends on the total number of gates are needed for an implementation. The single bit LSB lower parts are designed by one bit wise OR gate in place of (l-1) logic gates as used in other traditional multiplier.

The power consumption of LSB lower parts and LSB upper parts are

$$P_{LSB\_Lower} = \frac{(l-1)}{2^{(l-1)}} \quad (1)$$

$$P_{LSB\_Upper} = 0.2 \quad (2)$$

The total power consumption of LSB part is obtained from equation (1) & (2) then

$$P_{LSB} = P_{LSB_{Lower}} + P_{LSB_{Upper}} \quad (3)$$

$$P_{LSB} = \frac{(l-1)}{2^{(l-1)}} + 0.2 \quad (4)$$

The total power consumption of the n-bit probabilistic multiplier is estimated by the sum of m-bit MSB part and l-bit LSB part.

$$P_{Multiplier} = P_{MSB} + P_{LSB} \quad (5)$$

$$P_{Multiplier} = m + \frac{(l-1)}{2^{(l-1)}} + 0.2 \quad (6)$$

$$P_{Multiplier} = m + 2^{-(l-1)} * (l-1) + 0.2 \quad (7)$$

The power consumption and power benefit of different multipliers are shown in Table.1. The power savings for the different bit widths of LSB parts of different multiplier is shown in Fig.3.

Table I. POWER CONSUMPTION AND BENEFITS OF A MULTIPLIER

Design	**Power Consumption (n-bit)**	**Power Benefits (% of watts)**
CONVENTIONAL MULTIPLIER	m*+l**	0%
TRUNCATED MULTIPLIER (TM)	m+0	100% (with high error)
IMPRECISE MULTIPLIER (IM)	$m + (2^{-(l-1)}) (l-1) + 0.5$	50%
ERROR TOLERANT MULTIPLIER (ETM)	$m + (2^{-(l-1)}) (l-1) + 0.4$	60% (approx)
PROPOSED MULTIPLIER (PM)	$m + (2^{-(l-1)}) (l-1) + 0.2$	80%

*m=n (MSB) and **l=n/2 (LSB)

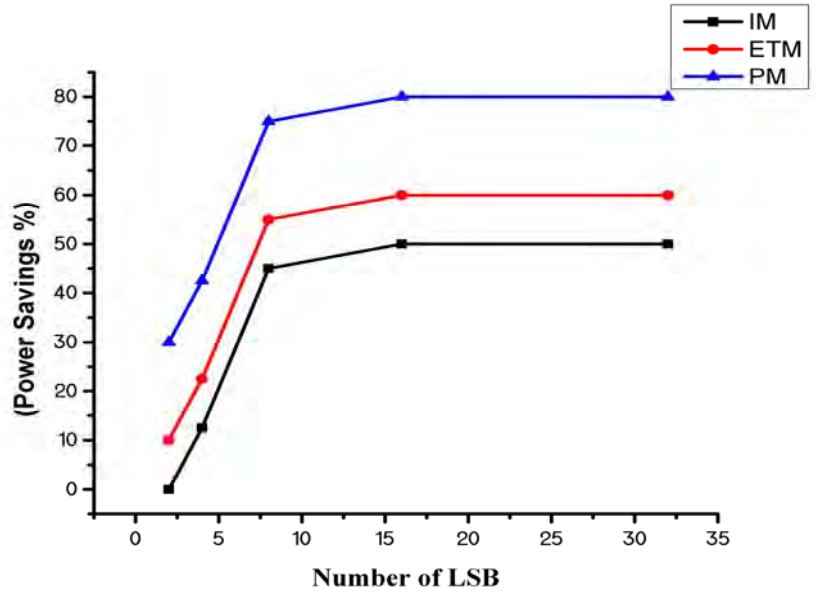

Fig.3. Power saving for the proposed multiplier

D. Error Calculation of the proposed Multiplier

All the errors are exponentially varying with LSBs. The error change depends on the LSBs of a multiplier. The overall performance of probabilistic multiplier can be described with different computation such as Error (e), Mean error ($\bar{e}$) and Absolute mean error ($|\bar{e}|$). The difference between the perfect result and imperfect result of the multiplier is called error function (e).

$$Error\ (e) = Perfect\ Result - Imperfect\ Result \qquad (8)$$

The mean error is

$$\bar{e} = \frac{1}{(2^n-1)^2} \left[\sum_{i=0}^{2^n-1} \quad \sum_{j=0}^{2^n-1} \left(P_{IJ} - P'_{IJ}\right)\right] \qquad (9)$$

where P_{ij} and P'_{ij} are the perfect and imperfect results of a multiplier for all possible input.

The mean values of multiple inputs are calculated by using mean absolute error. The mean absolute error is given by

$$|\bar{e}| = \frac{1}{(2^n-1)^2} \left[\sum_{i=0}^{2^n-1} \sum_{j=0}^{2^n-1} \left(|P_{ij} - P'_{ij}|\right)\right] \qquad (10)$$

The mean absolute error for various multipliers as a function of different LSB is shown in Fig.4. From the figure, it is understand that the proposed multiplier is better than that of other multiplier in terms of mean absolute error. The mean absolute error is reduced in the higher bit length of the multiplier. The aim of the proposed design is to minimize the power with sacrificing some reasonable accuracy.

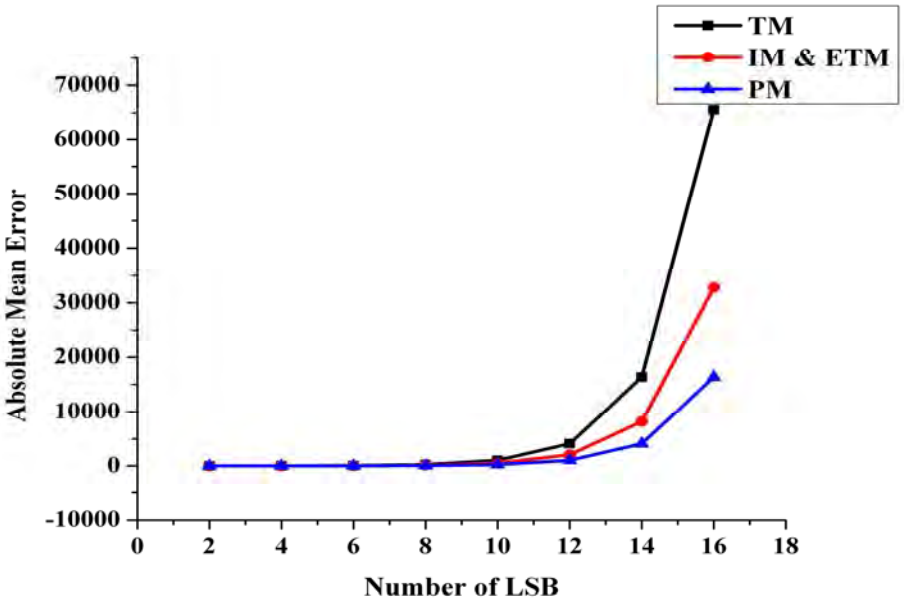

Fig.4. Mean Absolute error for different multiplier

Table.2 shows the error estimation of TM (Truncated Multiplier), IM (Imprecise Multiplier), ETM (Error Tolerant Multiplier) and the proposed PM (Probabilistic Multiplier). Truncated multiplier has to obtain maximum power benefits with high absolute mean error. Imprecise multiplier has the low power consumption and smaller delay; however, the transistor count is high. The absolute mean error of the ETM is high because of complex design of the inaccurate multiplier. The probabilistic multiplier gives better performance in terms of power consumption, delay and transistor count with minimum absolute mean error.

Table II. THE ERROR CALCULATIONS FOR DIFFERENT MULTIPLIER

Different Types of Multiplier	**Mean Error ($\bar{e}$)**	**Absolute Mean Error ($\lvert\bar{e}\rvert$)**	**Absolute Maximum Error ($\max\{\lvert\bar{e}\rvert\}$)**
TRUNCATED MULTIPLIER	$1-2^{LSB}$	$2^{LSB}-1$	$2^{LSB+1}-2$
IMPRECISE MULTIPLIER	$1/2-2^{LSB+1}$	$2^{LSB-1}-1/2$	$2^{LSB}-1$
ERROR TOLERANT MULTIPLIER	$2/3-2^{LSB-1}$	$2^{LSB-1}-2/3$	$2^{LSB}-4/3$
PROPOSED MULTIPLIER	$1/4-2^{LSB-2}$	$2^{LSB-2}-1/4$	$2^{LSB-1}-1/2$

III. RESULTS AND DISCUSSIONS

The proposed multiplier is designed and simulated using ISEsim. HSPICE software was used to construct the models of the 8-bit proposed and other multipliers. The total delay is calculated as the sum of LSB part delay and the MSB part delay. The 8 bit probabilistic multiplier with equal LSB part and MSB part reduces more area with minimum error, when compared to other conventional multipliers. 1000 sets of inputs were randomly created using the MATLAB program. The different possibilities of random inputs are given into the proposed multiplier circuit to obtain the simulated output and recorded the power consumption. The transistor count was derived openly from the HSPICE software.

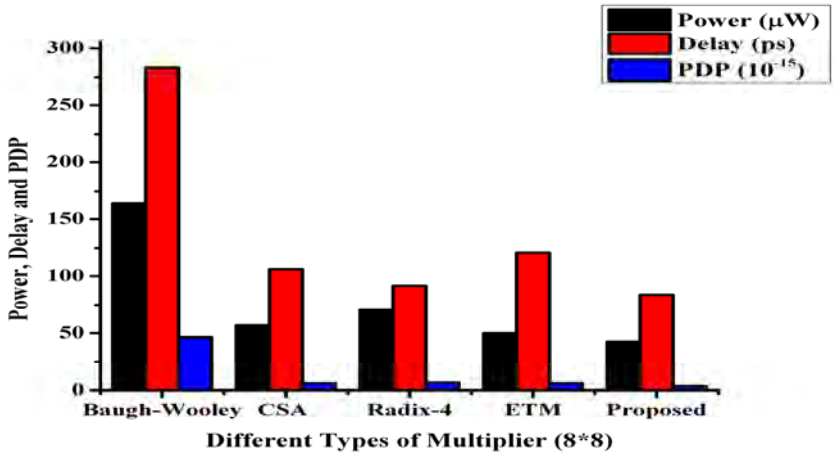

Fig.5. Power and delay for different types of multiplier

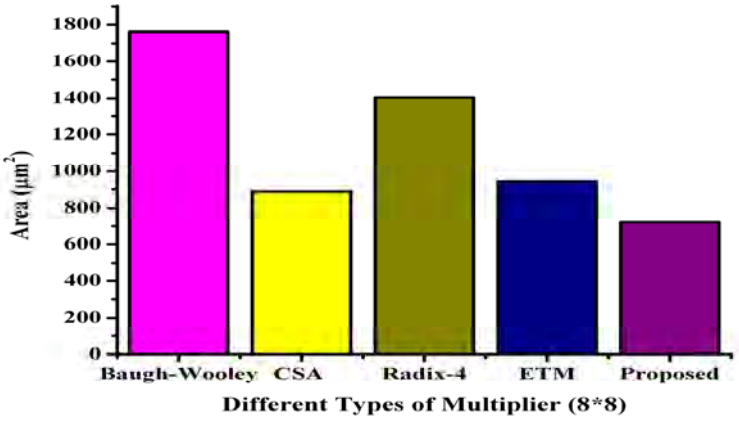

Fig.6. Area for different types of multiplier

The power dissipation and delay of the 8 bit proposed and other multipliers are shown in Fig.5. To compare the output of 8-bit proposed multiplier with actual value for 1000 number of samples, it is found that the average percentage of error is 1.25 i.e. the percentage of accuracy is 98.75%. Comparing the simulation and synthesis results of the proposed multiplier with those of other multipliers, it is evident that the proposed multiplier performed the best in terms of power consumption, delay and transistor count with less accuracy. From the Fig.6, it is very clear that the proposed probabilistic multiplier has less transistor count compared with other type of multipliers.

IV. Conclusion

The probabilistic design of power efficient multiplier has to obtain high power saving for the reduction of partial product generation. To reduce major power consumption of a multiplier design it is a good direction to reduce number of gates thereby reducing a dynamic power which is a major part of total power dissipation. The different error metrics are discussed and the simulation results are recorded. The applications of these multipliers are used in image processing and multimedia system fields. In future, the adaptive compensation circuits are designed and implemented in multiplier for different accuracy trade off. The proposed probabilistic multipliers are integration into FPGA signal processing blocks.

References

[1] L.D. Van and C.C. Yang, "Generalized low-error area-efficient fixed width multipliers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 8, pp. 1608–1619, Aug. 2005.

[2] T Oscal, C Chen, S Wang, and Y W Wu, "Minimization of Switching activities of partial products for designing low-power multipliers," *IEEE Trans. VLSI Systems.*, vol. 11, no. 3, pp. 418–433, 2008.

[3] M.C. Wen, S.J. Wang, and Y.N. Lin, "Low-power parallel multiplier with column Bypassing," *Electronic Letters.*, vol. 41, no.10, May. 2005.

[4] L.D.Van and J.H. Tu, "Power efficient pipelined reconfigurable fixed-width baugh-wooley multipliers," *IEEE Trans. Comput.*, vol. 58, no.10, pp. 1346–1355, Oct. 2009.

[5] S.R. Kuang and J.P. Wang, "Design of power-efficient configurable booth multiplier," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 3, pp. 568–580, Mar. 2010.
[6] S.R. Kuang J.P. Wang, and C.Y. Guo, "Modified booth multipliers with a regular partial product array," *IEEE Trans. Circuits Syst. II*, vol. 56, no. 5, pp. 404–408, May. 2009.
[7] R.S. Waters, and E.E. Swartzlander, "A Reduced Complexity Wallace Multiplier Reduction" *IEEE Trans. Computer*, vol. 59, no. 8, pp. 1134–1137, Aug. 2010.
[8] Jung-Yup Kang and Jean-Luc Gaudiot, "A simple high-speed multiplier design," *IEEE Trans. Comput.*, vol. 55, no. 10, pp. 1253–1258, Oct. 2006.
[9] C.H. Chang, and R.K. Satzoda, "A low error and high performance multiplexer-based truncated multiplier," *IEEE Trans. VLSI Systems.*, vol. 18, no. 12, pp. 1767–1771, Dec. 2008.
[10] H.J. Ko, and S.F. Hsiao, "Design and application of faithfully rounded and truncated multipliers with combined deletion, reduction, truncation, and rounding," *IEEE Trans. Comput.*, vol. 58, no. 5, pp. 304–308, May. 2011.
[11] H.Cho, L.Leem, and S. Mitra, "ERSA: Error resilent system architecture for probabilistic applications," *IEEE Trans. CAD of Integrated Circuits and Systems*, vol. 31, no. 4, pp. 546–558, 2012.
[12] I.P. Wang, S.R. Kuang, and Y.C. Chuang, "Design and error-tolerance in the presence of massive numbers of defects," *IEEE Des. Test. Comput.*, vol. 24, no. 3, pp. 216-227, May. 2004.
[13] K.Y. Kyaw, W. L. Goh, and K. S. Yeo, "Low power high- speed multiplier for error-tolerant application," in *Proc. IEEE Intel Conf. of EDSSC'10*, 2010, pp. 1 - 4.
[14] P. Kulkarni, P. Gupta, and M. Ercegovac, "Trading accuracy for power in a multiplier architecture," *J. Low Power Electron.*, vol.7, no. 4, pp. 490-501, 2011.
[15] P. Kulkarni, P. Gupta, and M. Ercegovac, "Trading accuracy for power with an under designed multiplier architecture," in *Proc. 24th Intel. Conf. on VLSI Design'11*, 2011, pp.346-351.
[16] J. Huang, J. Latch, and G. Robins, "A methodology for energy-quality tradeoff using imprecise hardware," in *Proc. DAC'12*, 2012, pp. 504 - 509.
[17] J. Huang, and J. Latch, "Exploring the fidelity-efficiency design space using imprecise arithmetic," in *Proc. ASPDAC'11*, 2011, pp. 579 - 584.
[18] D. Shin, and S. K. Gupta, "A new circuit simplification method for error tolerant applications," in *Proc. DATE'11*, 2011, pp. 1 - 6.
[19] I.P. Wang, S.R. Kuang, and Y.C. Chuang, "Design of reconfigurable low-power pipelined array multiplier," in *Proc. Int. Conf. Commun., Circuits. Syst.*, 2006, vol. 4, pp. 2277 - 2281.
[20] International Technology Roadmap for Semiconductors [Online]. Available: http://publich.itrs.net