Selective Harmonic Elimination of Five-level Cascaded Inverter Using Particle Swarm Optimization

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***Abstract*— This paper presents an efficient selective harmonics elimination method for a cascaded five-level inverter by using Particle Swarm Optimization (PSO) method. The aim of this research is to eliminate selected low-order harmonics by solving non-linear equations using the developed PSO algorithm, while at the same time the fundamental component is retained efficiently. In order to find the efficient switching angles of a five- level cascaded inverter, a PSO algorithm has been developed to solve the non-linear equations. Instead of single switching, multiple switching in a quarter cycles has been introduced to increase the number of harmonic orders that should be eliminated. With the proposed method, the required switching angles are computed efficiently by PSO in order to eliminate low-order harmonics up to the 17th order from the inverter voltage waveform. The entire system has been simulated using PSIM software and a prototype of five -level cascaded inverter with Field Programmable Gate Array (FPGA) has been built in the laboratory. Performance of the proposed method for a five-level cascaded H-bridge inverter, based on simulation studies, is evaluated and experimentally verified.**

Keyword- Selective Harmonic Elimination, Five-level Inverter, Field Programmable Gate Array, Particle Swarm Optimization

I. INTRODUCTION

In recent year, multilevel inverters have received more attention because of their ability to generate high quality output waveforms with low switching frequency. It is also have drawn great research interest and have been studied for several high-voltage and high-power applications [1]-[3]. Compared to conventional two level inverters, multilevel inverters have attracted a great deal of attention in medium-voltage and high-power applications due to their lower switching losses, high efficiency and more electromagnetic compatibility [4]-[7]. With multilevel inverter, as numbers of levels are increased, the output voltage steps generating waveform increased synchronously and at the same time the harmonic distortions are decreased.

In order to achieve the satisfactory performance of the operation, various power circuits have been proposed with modifications in the traditional inverter circuits [8]-[10]. Among the modified topologies, multilevel inverters have been considered as an optimum choice to provide better quality power to the load. There exist three most important multilevel inverter topologies: diode clamp [11], flying capacitor [12], and cascaded multilevel inverter with separate dc sources [13]. Among the above multilevel inverter structures, H-bridge or cascaded multilevel inverters are particularly attractive. It is because of their modularity and simplicity of control. Promising modulation scheme for cascaded multilevel inverters is staircase modulation which was proposed by J.Chiasson and L. M. Tolbert [14]. However there are active researches are being carried out by various researchers in the modulation schemes of inverters to provide better operating performances for different applications [15]-[19].

A variety of pulse width modulation (PWM) schemes commonly used for the cascaded multilevel inverters are based on the following methods: 1) sinusoidal PWM (SPWM); 2) space vector PWM (SVPWM); 3) non-sinusoidal carrier PWM; 4) mixed PWM; 5) special structure of cell connections and 6) selective harmonic elimination PWM (SHEPWM). Since multilevel inverters are usually operated with low switching frequency, SHEPWM offers several advantages over the other methods such as low switching frequency with a wider converter's bandwidth, direct control over low-order harmonics and better dc source utilization [20]-[27]. SHEPWM is also the most famous switching strategy that is widely used to specifically eliminate the selected order harmonics from the output waveform of the inverter. The main objective of the selective harmonic elimination is to eliminate or minimize the low-order harmonics or the harmonics close to the fundamental.

In order to eliminate the selected low- order harmonics from the output voltage/current waveform of a cascaded multilevel inverter, appropriate switching angles must be calculated and the power switching devices

has to be switched accordingly. To find these switching angles the transcendental equations derived from the Fourier series expansion of the output voltage of the inverter must be solved. Most of the recently reported research activities on selective harmonic elimination techniques; the transcendental equations were solved by Newton-Raphson or genetic algorithms (GA). In Newton-Raphson method they need a good initial guess that should be very close to the exact solution. Although the Newton-Raphson method works properly if a good initial guess is available, providing a good guess is very difficult in most cases [7]. This is because the search space of the SHE problem is unknown and one does not know whether a solution exists or not and if exists, what is the good initial guess. GA has been used to obtain optimal solutions for inverter. Despite their effectiveness in SHE, they are complicated and their parameters such as crossover and mutation probability, population size and number of generations are usually selected as common values given in literature or by means of a trial and error process to achieve the best solution set [28]. To overcome this problem PSO has been adopted in this study.

This paper presents the angle computation with PSO algorithm and the hardware implementation of five-level cascaded multilevel inverter using Field Programmable Gate Array (FPGA). With the proposed method, the required switching angles are computed efficiently by PSO in order to eliminate low-order harmonics up to the 17th order from the inverter voltage waveform. The proposed algorithm results better harmonic profile of the overall inverter system.

II. CASCADED FIVE-LEVEL INVERTER

The power circuit of a five-level cascaded inverter is shown in Fig. 1. Cascaded multilevel inverter is based on series connection of single phase H-bridge inverters with separate DC sources. The modular structure of cascaded multilevel inverter leads less space occupancy than other topologies. This topology requires less number of components compared to the flying capacitor and diode clamped multilevel inverter topologies. In addition to the above, cascaded multilevel inverter does not require a specially designed transformer as like in the multiphase inverters.

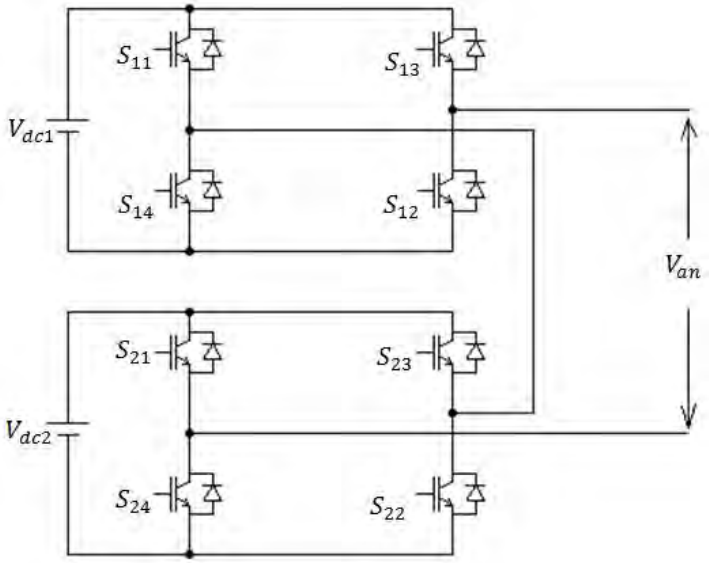


Fig. 1. Cascaded five-level inverter

Each H-bridge shown in Fig. 1 could produce three different levels: $+V_{dc}$, 0 and -V_{dc} by connecting the DC supply to AC output side by different combinations of the four switches S_{X1}, S_{X2} , S_{X3}, and S_{X4}, where X represents the H-bridge number. To obtain +V_{dc}, S_{X1} and S_{X2} switches are turned on. While for – V_{dc} level S_{X3} and S_{X4} are turned on. The output voltage would be made zero while switching on either the switch pairs S_{X1} and S_{X3} or S_{X2} and S_{X4} . The output voltage representation of a five-level cascaded inverter at fundamental switching frequency scheme is shown in Fig. 2. The number of levels (*m*) in the output phase voltage is *2s+1* where *s* is the number of H-bridges used. To obtain three phase connection, the outputs of three single phase inverters could be connected in star or delta shape.

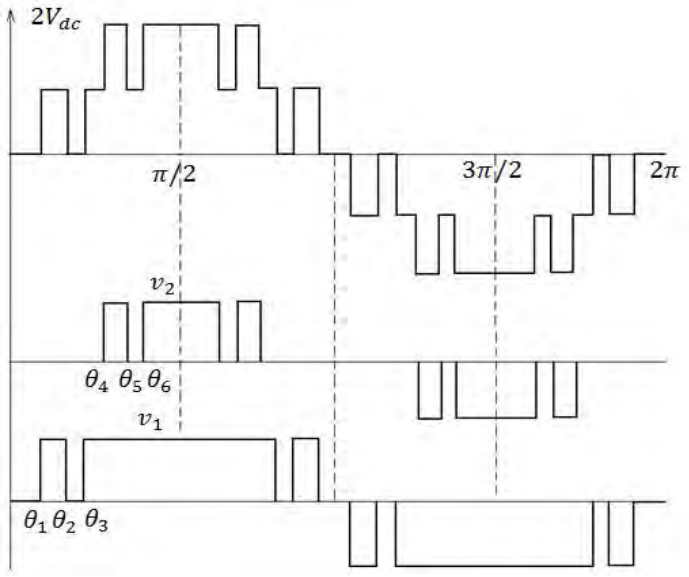


Fig. 2. Five-level phase voltage output

III. SELECTIVE HARMONIC ELIMINATION PWM

Generally a staircase pattern of the voltage waveform is being chosen for the selective harmonic elimination pulse width modulation (SHEPWM) in multilevel inverters. The number of switching angles in a quarter cycles is limited to *s* in the staircase voltage waveform. In this method, the number of harmonics that can be eliminated is limited to *s-1*. To overcome this problem, this paper proposes a multiple switching scheme in a quarter of a cycle in order to increase the number of harmonics that could be eliminated. The number of harmonic that could be eliminated is (*p x s)-1*.Where *p* is number of switching angles at each level. For five-level inverter and *p=3*, there are five undesired low- order harmonics could be eliminated. In this case 5^{th} , 7^{th}, 11^{th}, 13^{th} and 17^{th} harmonic could be eliminated efficiently. Considering Fig. 2, with equal DC sources amplitude, the Fourier series expansion of this waveform is:

$$V(\omega t) = \sum_{n=1,3,5..}^{\infty} \frac{4V_{dc}}{n\pi}\left(\cos n\theta_1 \pm cosn\theta_2 \ldots \pm\ cosn\theta_{ps}\right)\sin\left(n\omega t\right) \quad (1)$$

The switching angles $\theta_1 - \theta_{ps}$ must satisfy the following condition:

$$0 \le \theta_1 \le \theta_2 \le \cdots \theta_{ps} \le \frac{\pi}{2} \quad (2)$$

In equation (1), the positive signs indicate the rising edges and negative signs indicate the falling edges of the voltage waveform. In this paper, a five-level cascaded inverter and *p=3* is chosen as a case study. Thus, with six angles as degrees of freedom, it is possible to satisfy the fundamental component and to eliminate five low-order harmonics i.e. 5^{th}, 7^{th}, 11^{th}, 13^{th} and 17^{th}. Elimination of triplen harmonics i.e 3^{rd}, 9^{th}, 15^{th} is not necessary for three phase system because these harmonics are eliminated automatically from line-line voltage. In other words, for five -level inverters with *p=3*, the following non-linear equation should be solved:

$$\begin{aligned}
(s\pi/4)M &= cos\theta_1 \pm cos\theta_2 \pm cos\theta_3 \ldots cos\theta_{ps} \\
0 &= cos5\theta_1 \pm cos5\theta_2 \pm cos5\theta_3 \ldots \pm cos5\theta_{ps} \\
0 &= cos7\theta_1 \pm cos7\theta_2 \pm cos7\theta_3 \ldots \pm cos7\theta_{ps} \quad (3) \\
0 &= cos11\theta_1 \pm cos11\theta_2 \pm cos11\theta_3 \ldots cos11\theta_{ps} \\
0 &= cos13\theta_1 \pm cos13\theta_2 \pm cos13\theta_3 \ldots cos13\theta_{ps} \\
0 &= cos17\theta_1 \pm cos17\theta_2 \pm cos17\theta_3 \ldots cos17\theta_{ps}
\end{aligned}$$

Where, M is modulation index and defined as:

$$M = \frac{V_1}{sV_{dc}}\left(0 \le M \le 1\right) \quad (4)$$

It is necessary to determine six switching angles, namely θ_1, θ_2, θ_3, θ_4, θ_5 and θ_6 such that the equation set (3) are satisfied.

IV. PARTICLE SWARM OPTIMIZATION

Particle swarm optimization (PSO) was developed by Kennedy and Eberhart in 1995, based on the social behaviors of animal swarms (e.g. bird blocks and fish schools) [29]. It is a very powerful tool for optimization of non-linear equations or functions. It is initialized with a population of random solution and searches for optima satisfying some performance index. It uses the number of agents (particles) that constitutes a swarm moving around in the search space looking for best solution. The simplified PSO technique is as follows:

At first, the variables of the objective function are randomized. By iterations, the *Pbest* (present best) and *Gbest* (global best) values are computed. The velocity vector *V* for variable θ is then computed by using the expressions:

$$V(n+1) = W \cdot V(n) + C_1 \cdot rand\big(Pbest - \theta(n)\big) + C_2 \cdot rand(Gbest - \theta(n)) \quad (5)$$

$$X(n+1) = X(n) + V(n+1) \quad (6)$$

Where C_1 and C_2 are constants within the range of 1 and 2, *Pbest, Gbest* and present θ are *Pbest, Gbest* and present values of variable θ respectively, *W* is the inertia weight, the value of which is chosen depending upon the type of problem and search criteria. A larger value of inertia weight *W* facilitates global exploration. While a smaller value of inertia weight tends to facilitate local exploration to fine tune the current search area. Proper selection of the inertia weight *W* can afford a balance between global and local exploration abilities and thus require less iteration on average to find the optima. The rand stands are random value uniformly distributed within [0, 1]. New Pbest and Gbest values of the variables are computed according to the equation (5). Finally, the non-linear equations converges at Pbest = Gbest after the extensive search. Unlike other iterative methods, the main advantage of this method is that there will be no initial guess for convergences required [30]. PSO also has better computational efficiency and exhibits more stable convergence characteristic than other optimization methods. A flowchart of the proposed PSO algorithm is shown in Fig.3.

V. RESULTS AND DISCUSSION

A. SIMULATION RESULTS

Multiple switching angles within a quarter of a voltage cycle have been calculated using the PSO algorithm. To validate the computational results for switching angles, a simulation is carried out in PSIM software tool for a five- level cascaded inverter. The DC source for each H-bridge unit is considered to be 48V and the simulation is carried out for *p=3* for different modulation indices. Phase voltage output waveform(single phase pattern), line-line voltage output waveform(three phase pattern) and frequency spectra of phase voltage and line-line voltage for modulation index 0.5 and modulation index 1 are shown in Fig.4 to Fig. 7 respectively. From the frequency spectra of phase voltage (Fig.4b and Fig. 6b), one can understand that the low- order non triplen harmonics such as 5^{th}, 7^{th}, 11^{th}, 13^{th} and 17^{th} are eliminated.

From the frequency spectra of line-line voltage(Fig. 5b and Fig. 7b), it can be also observed that the low-order harmonic including triplen harmonic up to 17^{th} harmonic are efficiently eliminated. Fig. 4 and Fig. 5 shows the simulation results for the modulation index 0.5 and the switching angles θ_1*=39.96°*, θ_2*=45.26°*, θ_3*=50.29°* θ_4*=72.56°*, θ_5*=77.67°* and θ_6*=84.67°* calculated by the proposed PSO algorithm. The phase voltage output waveform for the above switching scheme is shown in Fig. 4a. In this scheme, in a quarter of a full output cycle, the first H- bridge is switched three instants at θ_1*=39.96°*, θ_2*=45.26°* and θ_3*=50.29°* and the second H-bridge is switched three instants at θ_4*=72.56°*, θ_5*=77.67°* and θ_6*=84.67°* and totally each inverter H-bridge is switched six times in a cycle. It ensures multiple switching and the corresponding frequency spectrum of the phase voltage has been shown in Fig. 4b. It is evident from the spectra, that the low- order non triplen harmonics such as 5^{th}, 7^{th}, 11^{th}, 13^{th} and 17^{th} are eliminated from the phase voltage waveform. However the third and fifteen order harmonic appears in the spectrum, because the triplen harmonics were not eliminated automatically in the single phase inverter system. Fig 5a shows the line-line voltage of the five-level cascaded inverter when switched nine times in a quarter of a full cycle. The corresponding frequency spectrum for nine switching instants per quarter of a full cycle has been shown in Fig. 5b. It could be observed that, the low- order harmonics in the frequency spectrum is disappeared and the fundamental is improved well.

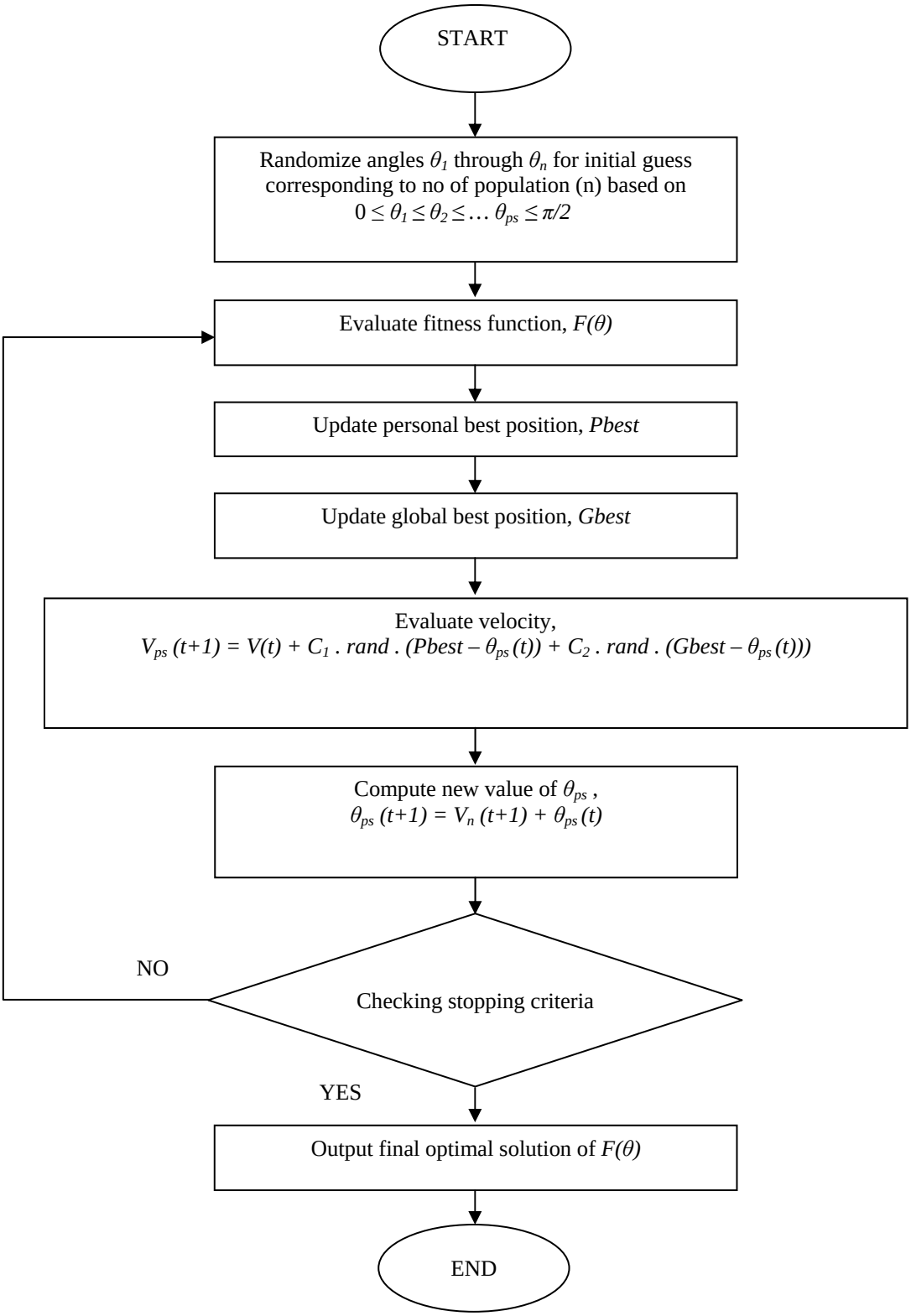
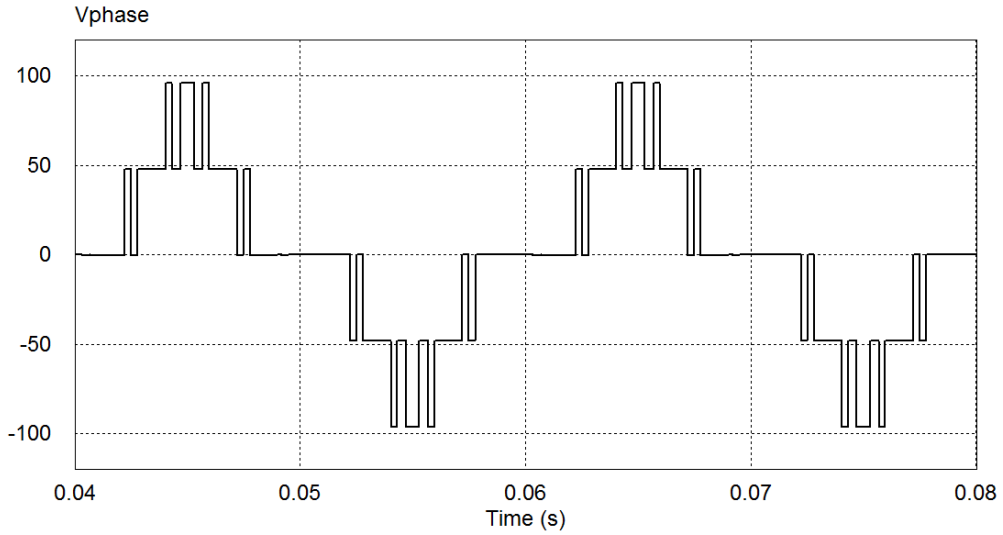


Fig. 3. Flowchart of proposed PSO algorithm

Extensive simulation study has been carried out for different set of multiple switching angles computed by the proposed PSO algorithm. Fig. 6a and 6b show the simulation results for phase voltage output waveform and frequency spectra of the phase voltage for the modulation index 1 when each inverter H-bridge is switched three instants. The switching angles for this case are $\theta_1=31.8°$, $\theta_2=36.92°$, and $\theta_3=46.32°$ for H-bridge I and $\theta_4=70.88°$, $\theta_5=78.82°$ and $\theta_6=85.41°$ for H-bridge II. Fig. 7a and 7b show the simulation results for line-line voltage output waveform and frequency spectra of the line-line voltage for the modulation index being maintained as 1.

From all the cases studied in the simulation, it is observed that the desired low- order harmonics are eliminated efficiently and eventually the total harmonic distortion (THD) of the output voltage is improved better than the traditional switching schemes. For example the output voltage THD of the five- level cascaded inverter using traditional switching scheme with modulation index 1 was found as 5.18% and the multiple switching scheme shown in Fig 7b was found as 0.302%. Therefore, the proficiency of the proposed multiple switching schemes using PSO algorithm is shown to be better than the conventional switching scheme.



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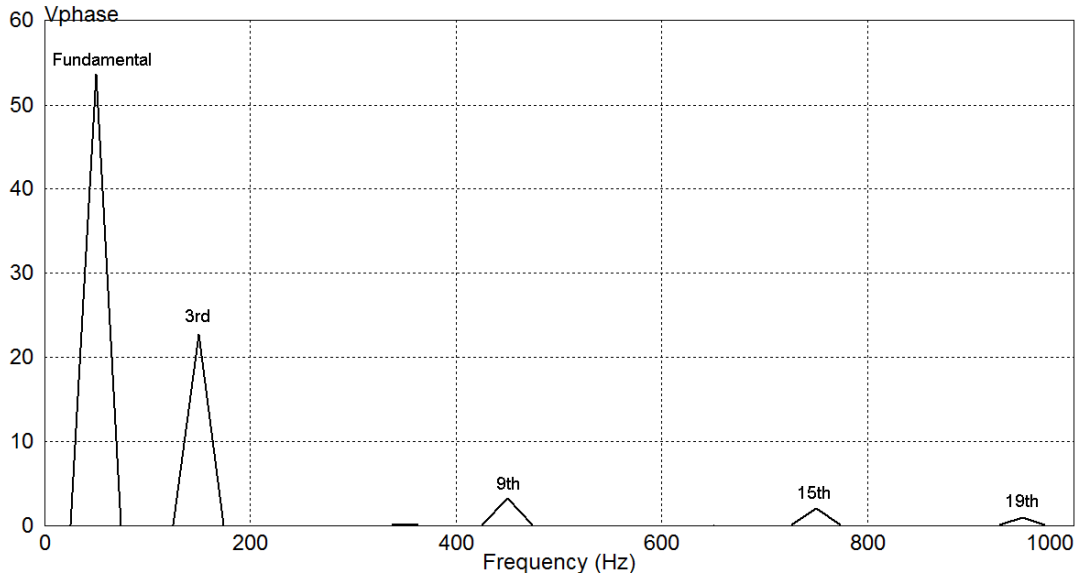

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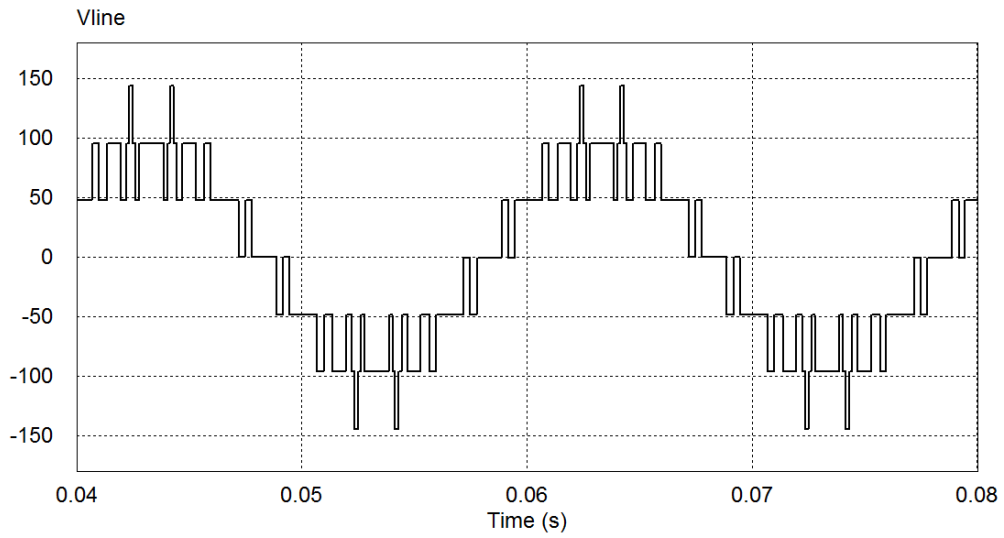
Fig. 4. Simulation results for modulation index =0.5 for single phase. (a) Phase voltage output waveform. (b) Frequency spectra of the phase voltage output waveform.



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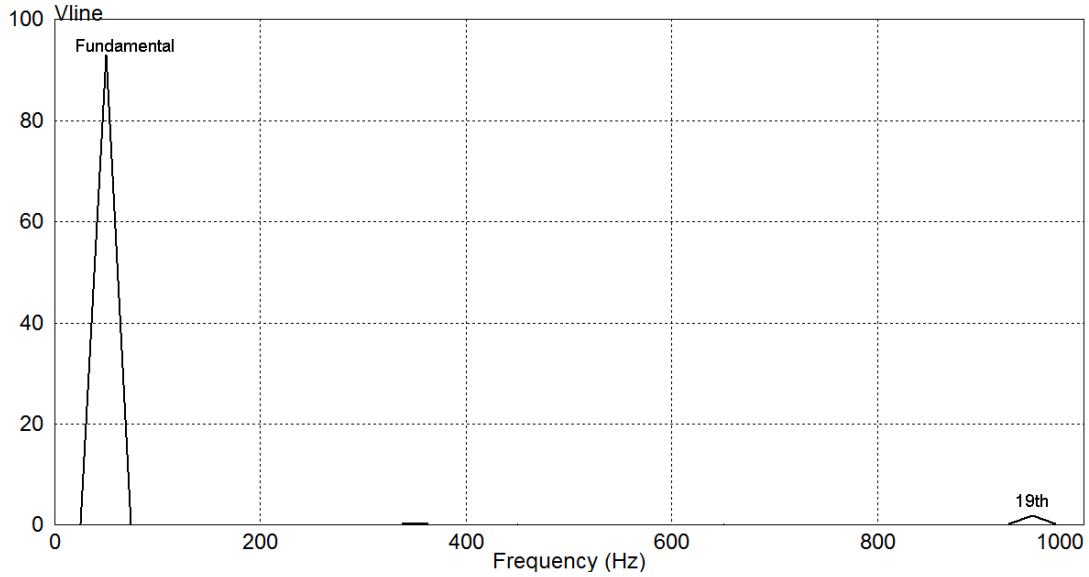

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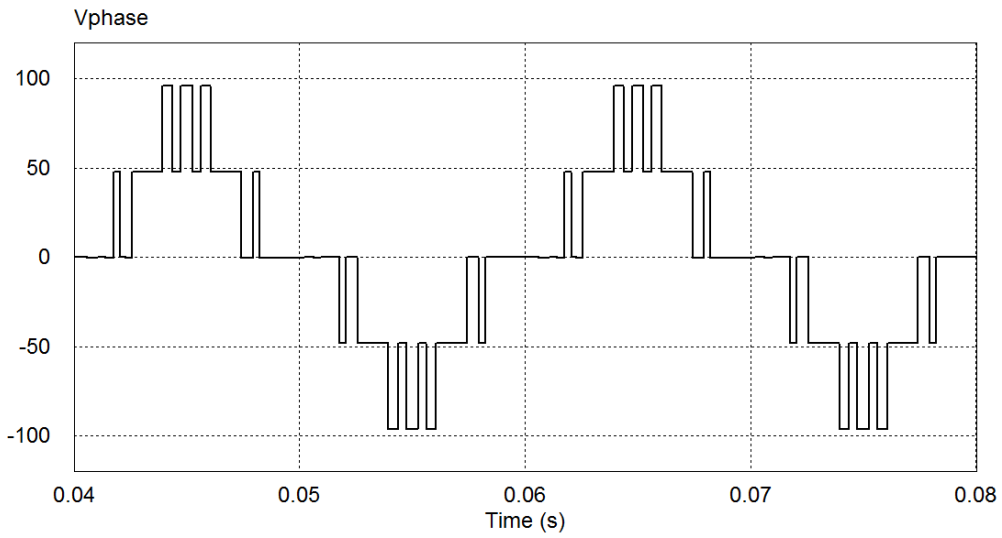
Fig. 5. Simulation results for modulation index =0.5 for three phase. (a) Line-line output waveform. (b) Frequency spectra of the line-line output waveform



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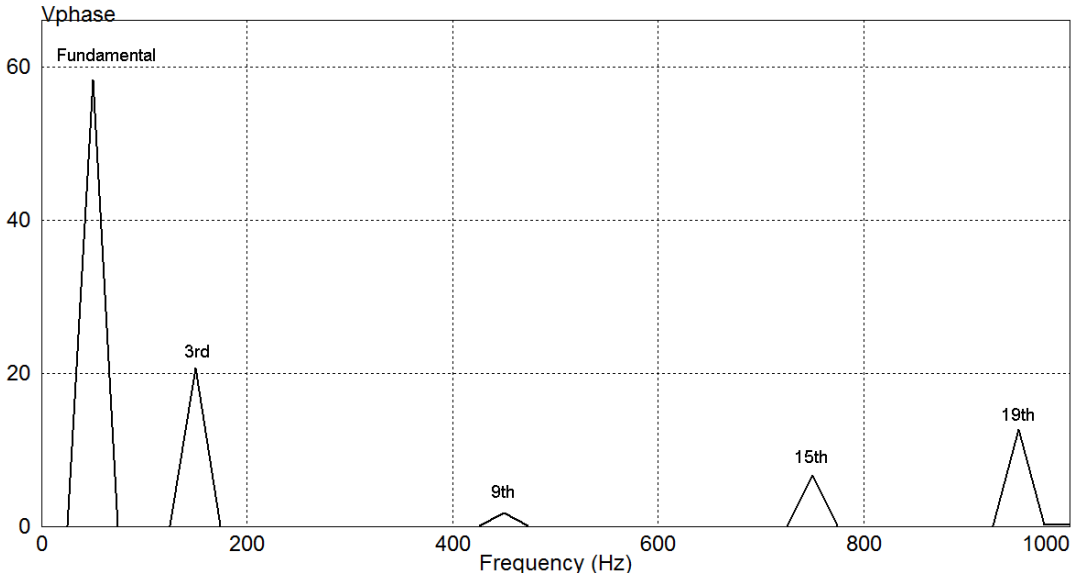

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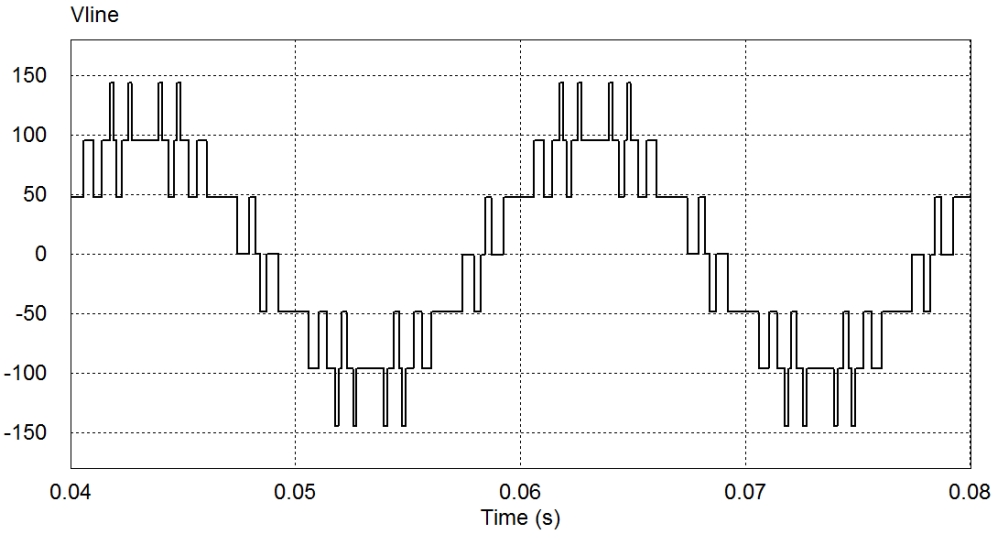
Fig. 6. Simulation results for modulation index =1 for single phase. (a) Phase voltage output waveform. (b) Frequency spectra of the phase voltage output waveform.



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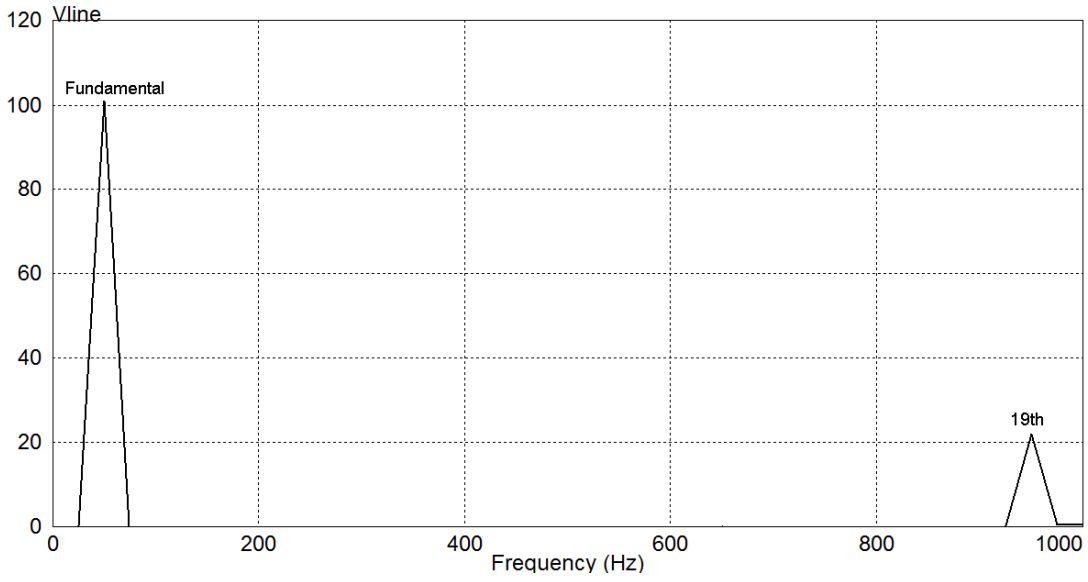


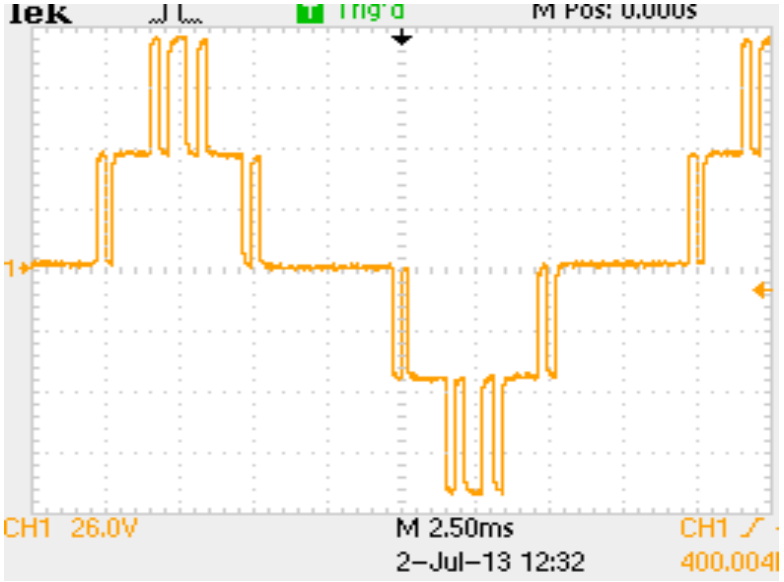
(b)

Fig. 7. Simulation results for modulation index =1 for three phase. (a) Line-line output waveform. (b) Frequency spectra of the line-line output waveform

B. EXPERIMENTAL RESULTS

To validate the results obtained in the simulations, a single phase five-level cascaded inverter prototype has been developed in the laboratory. Two switching H-bridges with power MOSFET IRFP250 with the rating of 200V/33A have been designed. The switching angles are obtained offline by the proposed PSO algorithm for the range of modulation indices as discussed in the simulations. The switching angles are implemented in DE0 Altera field programmable gate array (FPGA) board. The crystal frequency of the FPGA is set to 50MHz (equal to $2X10^{-8}$seconds) for fast and reliable operation. Then the counter value is set to 1,000,000 counts for $2x10^{-8}$ seconds and the appropriate switches are made ON and OFF for certain intervals depending upon the switching angles to be applied. Through the FPGA board, it transfers the switching pulses to the gates of the power MOSFET through an optocoupler A3180 in order to provide isolation for power MOSFET from the FPGA. The switching pulses are then transferred to power MOSFET driver that is connected to MOSFET and supplies 15V that is required for turning MOSFET ON. A 15 volt DC supply is designed using step-down transformer based diode rectifier system. Two separate 48V DC supplies have been used to power the H-bridges, these DC supplies could be either from AC mains through diode rectifier system or non-conventional power source means such as photovoltaic arrays, wind mills and fuel cells. In this research, a front end diode rectifier system has been used. A digital storage oscilloscope of Tektronik TPS 2014, was used for recording the output voltage waveform and Total Harmonic Distortion (THD).

In order to verify the simulation results the experimental is done for *p=3* for different modulation indices as done in the simulations. Phase voltage output waveform and frequency spectra of phase voltage for modulation index 0.5 and modulation index 1 are shown in Fig. 8 through Fig. 9. From the experimental results, it is seen that the low- order harmonic 5^{th}, 7^{th}, 11^{th}, 13^{th} and 17^{th} are efficiently eliminated as obtained in the simulations. In all the cases, the results obtained in the experiment agree with the simulation results. The response of the output voltage THD with respect to different modulation indices from 0.25 to 1 for all the low-order harmonics have been depicted in Fig. 10. From the graph one could observe that, all the desired low-order harmonics such as 5^{th}, 7^{th}, 11^{th}, 13^{th} and 17^{th} orders are less than 1% of the fundamental and close to zero. The values of the calculated switching angles for different values of modulation indices have been shown in Fig. 11.



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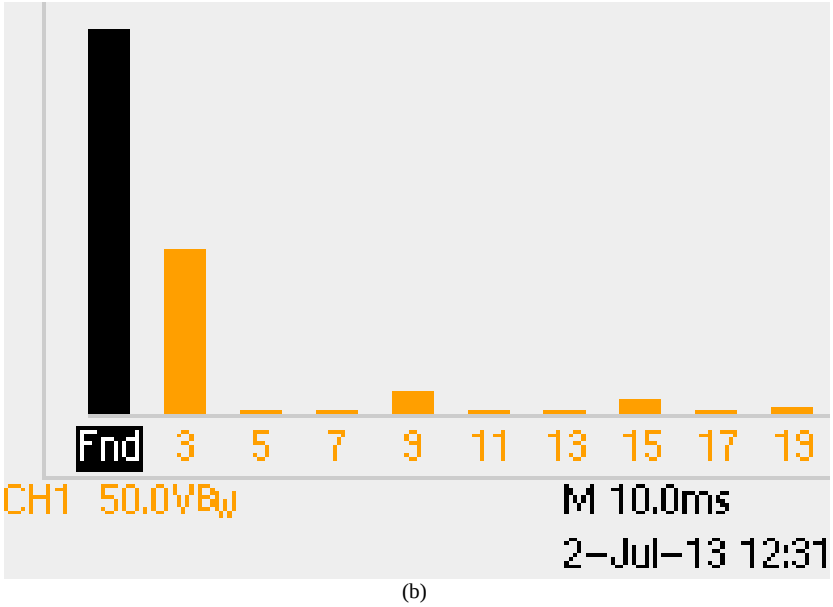

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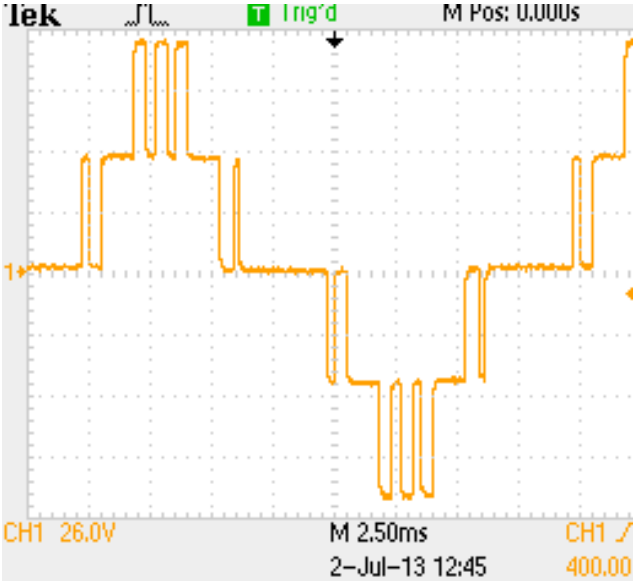
Fig. 8. Experimental results for modulation index =0.5 for single phase. (a) Phase voltage output waveform (b) THD profile of the phase voltage output waveform.



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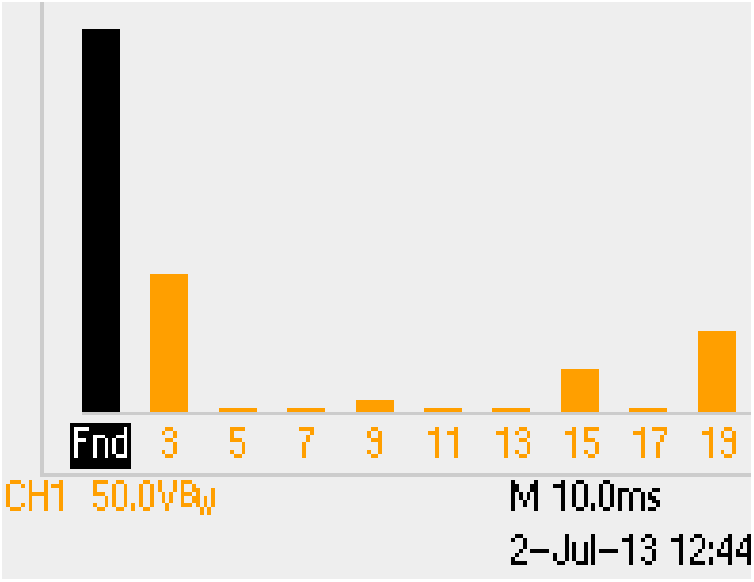

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Fig. 9. Experimental results for modulation index =1 for single phase. (a) Phase voltage output waveform (b) THD profile of the phase voltage output waveform.

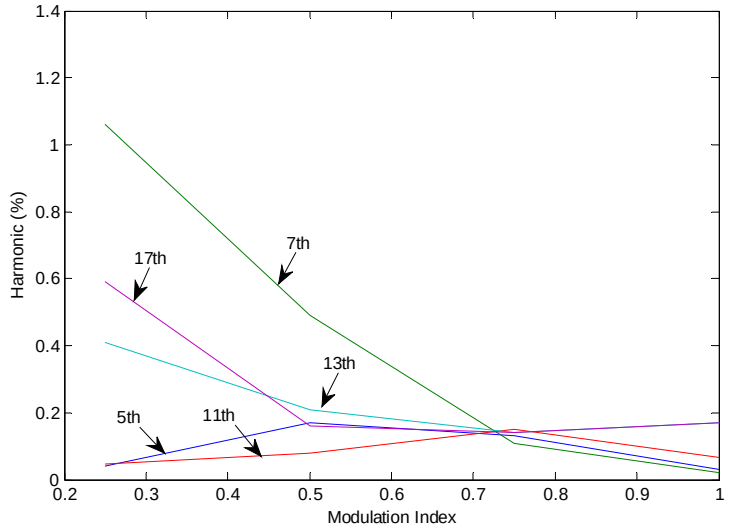

Fig. 10. Percentages of low-order harmonics

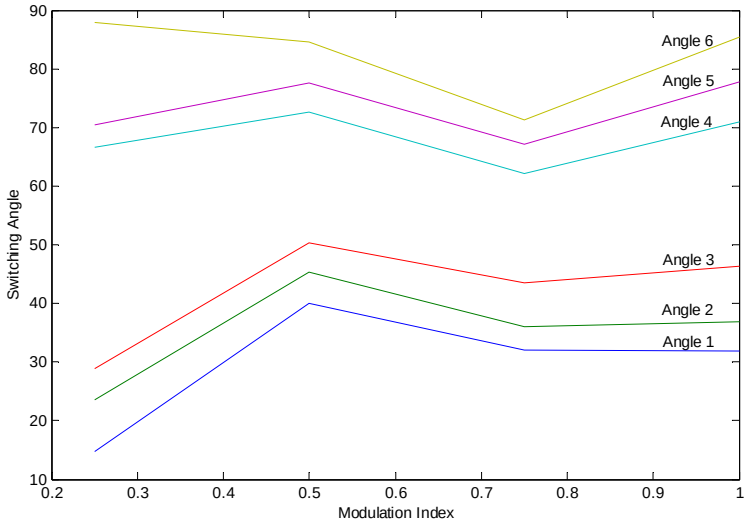

Fig. 11. Switching angles versus modulation index

VI. CONCLUSION

In this paper, elimination of desired low-order harmonics using SHEPWM strategy is investigated. Multiple switching angles have been calculated by solving the non-linear equation using PSO algorithm. With the proposed method, the low- order harmonics could be eliminated up to 17^{th} for the five-level cascaded inverter. The programming language has been described in Verilog and synthesised using Quartus II software before being implemented in Altera FPGA board. It was then applied to the gates of the power MOSFET. The entire model has been simulated using PSIM software and a single phase five-level inverter prototype has been developed in the laboratory. The experimental results are closely agreed with the simulation results for all the cases studied in this paper.

ACKNOWLEDGMENT

The authors would like to thank Ministry of Education for financially supported under MTUN COE grant number 9016-00007.

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