

# Folded Low Resource HARQ Detector Design and Tradeoff Analysis with Virtex 5 using PlanAhead Tool

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**Abstract**—Physical Hybrid Automatic Repeat reQuest (HARQ) Indicator Channel (PHICH) is used to report the correct reception of the uplink user data to the User Equipment (UE) in the form of Acknowledgment (ACK) or Negative ACK (NACK). In Long Term Evolution –Advanced (LTE-A) base station and UE have multiple antenna ports to provide transmit and receive diversities. An algorithm for decoding the HARQ value at UE is designed using maximum likelihood (ML) and maximal ratio combining (MRC) methods. Further, novel low complexity receiver architectures based on the VLSI Digital Signal Processing (DSP) techniques - folding method and parallel processing with folding method to reduce the operational units is proposed to reduce resource consumption. Tradeoff analysis of the proposed structures in terms of the timing cycles, operational resource requirement and resource complexity is discussed. The proposed system is optimal compared to other possible ways as it employs parallel processing with folding approach. It is a suitable solution for the area optimized hardware implementation of physical downlink channel receiver structures LTE-A whose delay results also meet the frame timing constraint. The proposed architectures are used to implement in Field Programmable Gate Array (FPGA) Virtex-5 xc5v1x50tff1136-1 device for single/multiple antenna configurations at base station and UE.

**Keyword**- LTE-Advanced, Spatial Diversity, Space Frequency Block Code, Folding, Parallel Processing

## I. INTRODUCTION

Long Term Evolution (LTE-A) is a fourth generation wireless broadband technology, which is capable of providing high peak data rates, multi antenna support, reduced cost and wide range of bandwidth. The LTE-A physical layer provides a highly efficient means of conveying data and control information between an enhanced base station (eNodeB) and mobile user equipment (UE). It uses OFDM along with MIMO antennas. It supports Frequency-Division Duplex (FDD) and Time-Division Duplex (TDD), as well as a wide range of system bandwidths [1]. LTE-A standard has six physical layer channels for downlink. The control signals are transmitted at the start of each sub-frame in the LTE-A grid. The Physical Broadcast channel (PBCH) carries the basic system information. The Physical Downlink Shared Channel (PDSCH) is the main data-bearing downlink channel in LTE-A. The Physical Multicast Channel (PMCH) is defined for future use. The Physical Downlink Control Channel (PDCCH) is mainly used to carry scheduling information of different types and uplink power control instructions. The Physical Control Format Indicator Channel (PCFICH) is transmitted on the first symbol of every sub-frame carrying the Control Format Indicator (CFI) field.

The Physical Hybrid ARQ (Automatic Repeat ReQuest) Indicator Channel (PHICH) is used to report the Hybrid ARQ (HARQ) status which indicates to the UE whether the uplink user data is correctly received or not. The 1 bit HARQ Indicator (HI) indicates "1" for positive acknowledgement (ACK) and "0" for Negative ACK (NACK). Multiple PHICHs are mapped to the same set of resource elements (REs). This set of REs constitutes a PHICH group. The PHICHs within a PHICH group are separated through different orthogonal sequences. A PHICH group is shared among eight UEs, by assigning each UE a different orthogonal sequence index. Together the PHICH group number and orthogonal sequence index are known as a PHICH resource.

The block diagram for the PHICH transmit and receive processing at the first User Equipment (UE) is shown in Fig. 1. Single bit ACK/NACK undergoes repetition coding [2], BPSK modulation and multiplication with spreading sequences. In LTE-A, 2M spreading sequences are used in a PHICH group, where  $M = 4$  for normal cyclic prefix (CP). The first set of  $M$  spreading sequences is formed by  $M \times M$  Hadamard matrix, and the second set of  $M$  spreading sequence is in quadrature to the first set. Hence each user has got an orthogonal sequence as shown in Table I, to be multiplied with the information to improve robustness. The channel carries

information of 8 users in 12 subcarriers. The 12 subcarriers generated for each user are superpositioned with that of the other 7 users and transmitted after LTE-A processing.

The transmitted signal endures the effect of channel gain and noise before reaching the receiver. At the receiver, the received signals after demapping and pre-processing with channel gain are again multiplied with orthogonal sequence of the specific user to get back the 12 subcarriers. Finally the HARQ indicator (HI) is detected from the decoded output based on the magnitude of the resulting value. Taking a 1.4 MHz bandwidth LTE system as an example, up to 7 OFDM symbols need to be processed within one slot (0.5 ms) which may contain 468 data subcarriers. This means that there will be no more than  $1.068\mu\text{s}$  to finish the detection of each subcarrier in average. Therefore, proper detection methods have to be chosen in order to maximize the data rate at reasonable implementation cost.

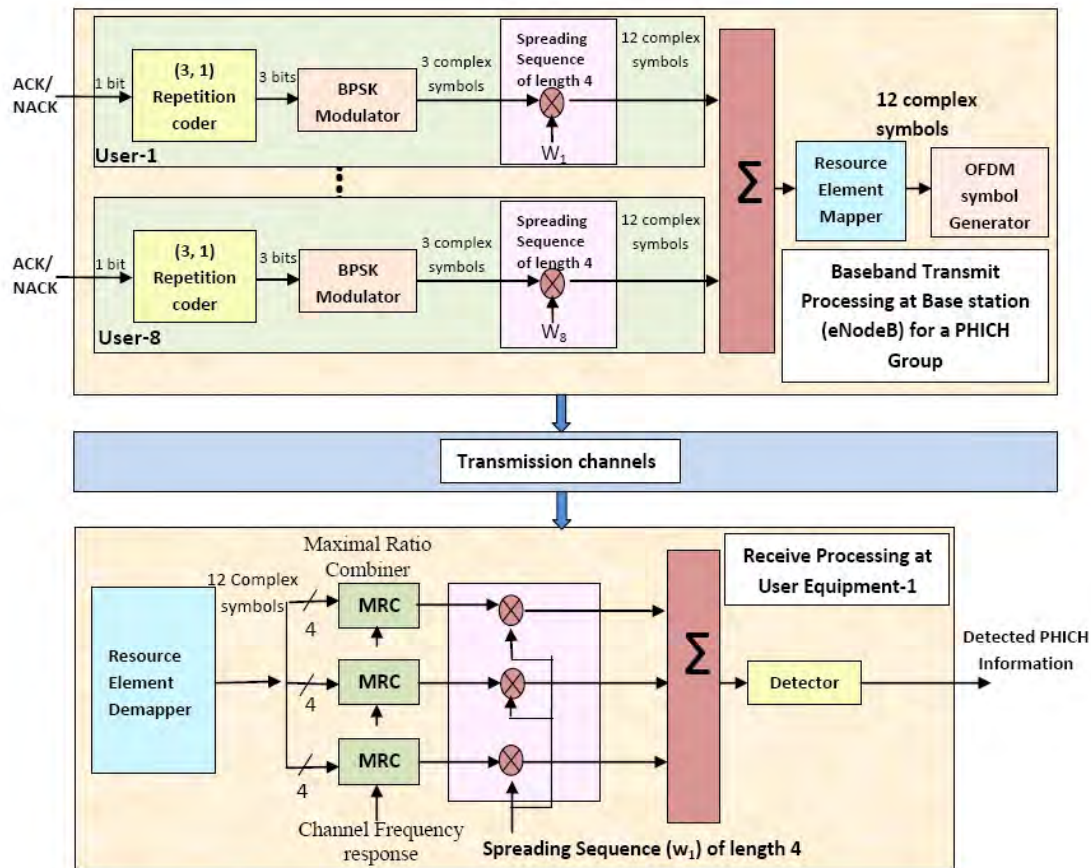


Fig. 1. Block diagram of transmit processing and receive processing for PHICH

TABLE I  
Orthogonal sequences for PHICH

Sequence index	Orthogonal sequence
User	Normal cyclic prefix
0	[+1 +1 +1 +1]
1	[+1 -1 +1 -1]
2	[+1 +1 -1 -1]
3	[+1 -1 -1 +1]
4	[+j +j +j +j]
5	[+j -j +j -j]
6	[+j +j -j -j]
7	[+j -j -j +j]

The objective of this paper is to synthesize and implement the receiver architecture of PHICH. The paper is structured as follows: Section 2 gives the system model architecture for Single Input Single Output (SISO) environment and Single Input Multiple Output (SIMO) environment. Section 3 gives the description of the system model architecture for Multiple Input Single Output (MISO) and Multiple Input Multiple Output (MIMO)

scenario. Section 4 discusses the implementation methods, section 5 discusses the simulation and implementation results and section 6 contains the concluding remarks.

**II. SYSTEM MODEL AND ARCHITECTURE FOR SISO AND SIMO CONFIGURATION**

The expression for signal received at the first UE is given by

$$y_1 = h_1 \circ (w_1 x_1 + \sum_{n=2}^M w_n x_n) + u_1 \tag{1}$$

where  $y_1=[y_{11}^T, y_{12}^T, y_{13}^T]^T$  is a (12x1) received signal vector with  $y_{11}=[y_0, y_1, y_2, y_3]^T$ ,  $y_{12}=[y_4, y_5, y_6, y_7]^T$  and  $y_{13}=[y_8, y_9, y_{10}, y_{11}]^T$ ,  $h_1=[h_{11}^T, h_{12}^T, h_{13}^T]^T$  is a (12x1) channel gain frequency response vector with  $h_{11}=[h_0, h_1, h_2, h_3]^T$ ,  $h_{12}=[h_4, h_5, h_6, h_7]^T$  and  $h_{13}=[h_8, h_9, h_{10}, h_{11}]^T$ , ‘ $\circ$ ’ represents the element by element multiplication and ‘ $u_1$ ’ is the (12x1) white Gaussian noise vector with unit variance and zero mean.  $w_n$  is (4x1) the spreading sequence vector of  $n^{th}$  UE in a PHICH group, obtained from the orthogonal set of codes.  $x_n$  is the 1 bit data value for acknowledge information of the  $n^{th}$  UE HI among 8 UEs. The objective is to detect  $x_1$  given  $y_1$  and assuming that  $h_1$  is known. Without loss of generality, it is assumed that the desired HI channel to be decoded uses the first orthogonal code denoted as  $w_1$ . By ML decoding at the UE-1 receiver [3],

$$z_1 = \sum_{i=1}^3 Re\left\{y_{1i} \circ h_{1i}^* w_1\right\} \tag{2}$$

$y_{1i}$  and  $h_{1i}$  are the  $i^{th}$  (4x1) received vector and its corresponding (4x1) channel frequency response vector.

Fig. 2 shows the basic architecture for SISO configuration which consists of three Receiver Processing Blocks (RPB) since there are 12 subcarriers in a column in each slot for PHICH. The internal architecture of RPB is shown in Fig. 3. RPB1 multiplies set of four received signals ( $y_{11}$ ) with conjugate values of channel frequency response ( $h_{11}$ ) and the output is multiplied with the receiver spread sequence to obtain the decoded output A. Hence 8 complex multiplications are involved.

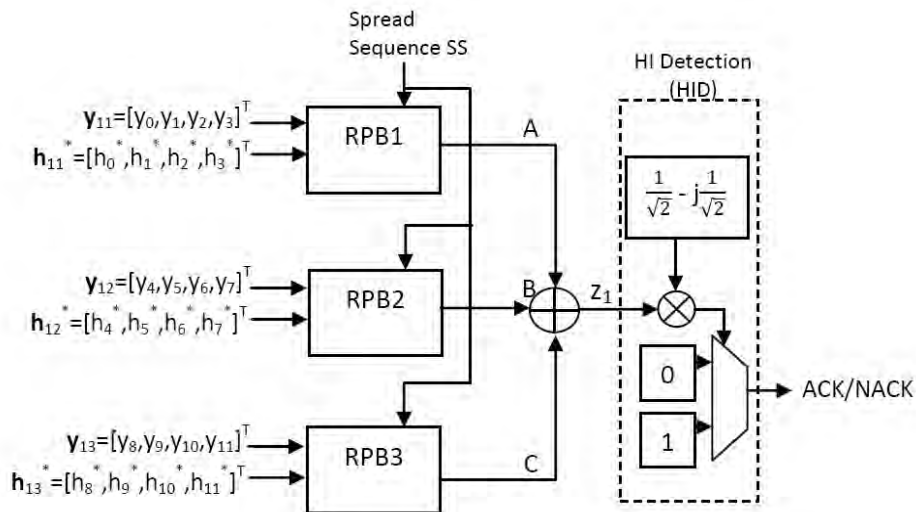


Fig. 2. Proposed SISO receiver architecture for PHICH

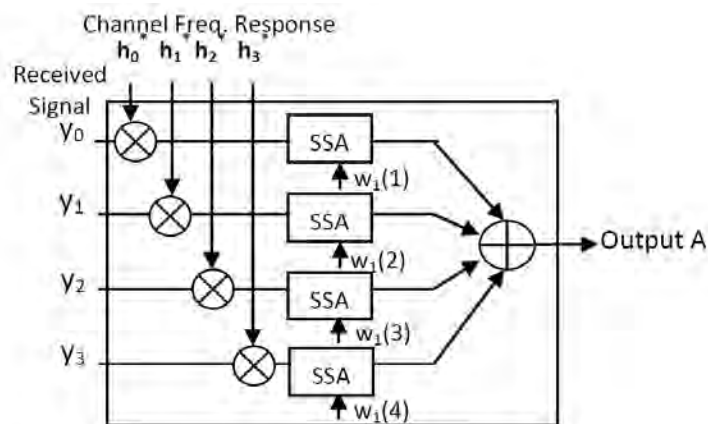


Fig. 3. Internal architecture for SISO Receiver Processing Block (RPB-1)

In order to reduce the complex multiplications, a Spread Sequence Assignment (SSA) block is proposed. The SSA consists of a multiplexer component with few registers. The complex valued results of  $(y_{1i} \circ h_{1i}^*)$  in (2) change according to the control variable 'cv'. The 'cv' value and its corresponding spread sequence multiplication component are given in Table II. The SSA block involves selection of the multiplexer output without requiring actual multiplication. This reduces the total complex multiplications by four. Similarly the RPB2 and RPB3 blocks process 4 received signals each ( $y_{12}$  and  $y_{13}$ ) with corresponding channel frequency response ( $h_{12}$  and  $h_{13}$ ) respectively. The output is multiplied with the receiver spread sequence to obtain decoded outputs B and C respectively. The sum of A, B and C is given to HI Detection (HID) block as shown in the Fig. 2 where it is multiplied with  $(1/\sqrt{2}) - j(1/\sqrt{2})$  and the magnitude of the real part is used for detecting  $x_1$ .

TABLE II  
Processing control in SSA block using 4:1 multiplexer

Spread Sequence Code bit	Multiplexer Control Variable (cv)	Description of SSA Output
+1	00	No change
-1	01	Change of Sign of real and imaginary parts
+j	10	Real and Imaginary parts are exchanged with sign change in real part
-j	11	Real and Imaginary parts are exchanged with sign change in imaginary part

In LTE-A, UE has maximum of 2 antenna ports to provide receive diversity. In SIMO processing, similar to (1), the complex-valued input to the  $k^{th}$  receive antenna of UE-2 is modelled as

$$y_2^{(k)} = h_2^{(k)} \circ \left( w_1 x_1 + \sum_{n=2}^M w_n x_n \right) + u_2^{(k)} \tag{3}$$

where  $k=0,1,2,\dots,K-1$  and  $K$  is the number of receive antennas at UE.  $y_2^{(k)}$  is  $(12 \times 1)$  received signal subcarrier vector,  $h_2^{(k)}$  is  $(12 \times 1)$  complex channel frequency response, and  $u_2^{(k)}$  represents the white Gaussian noise vector with unit variance and zero mean. Without loss of generality, it is assumed that the desired HI channel to be decoded uses the second orthogonal code denoted as  $w_2$ . According to ML decision rule, the decision statistic  $z_2$  for SIMO is:

$$z_2 = \sum_{i=1}^3 \sum_{k=0}^{K-1} Re \left\{ \left\langle y_{2i}^{(k)} \circ h_{2i}^{(k)*}, w_2 \right\rangle \right\} \tag{4}$$

where  $y_{2i}^{(k)}$  is the  $i^{th}$   $(4 \times 1)$  received vector with  $y_{21}^{(k)} = [y_0^{(k)}, y_1^{(k)}, y_2^{(k)}, y_3^{(k)}]$ ,  $y_{22}^{(k)} = [y_4^{(k)}, y_5^{(k)}, y_6^{(k)}, y_7^{(k)}]$ ,  $y_{23}^{(k)} = [y_8^{(k)}, y_9^{(k)}, y_{10}^{(k)}, y_{11}^{(k)}]$  and  $h_{2i}^{(k)}$  is its corresponding  $i^{th}$   $(4 \times 1)$  channel frequency response vector with  $h_{21}^{(k)} = [h_0^{(k)}, h_1^{(k)}, h_2^{(k)}, h_3^{(k)}]^T$ ,  $h_{22}^{(k)} = [h_4^{(k)}, h_5^{(k)}, h_6^{(k)}, h_7^{(k)}]^T$ ,  $h_{23}^{(k)} = [h_8^{(k)}, h_9^{(k)}, h_{10}^{(k)}, h_{11}^{(k)}]^T$ .

The SIMO 1x2 architecture shown in the Fig. 4 has two sets of SISO processing blocks RPB<sup>(0)</sup> and RPB<sup>(1)</sup> for manipulation of signals received at Antenna '0' and Antenna '1' respectively. The internal structure of receiver processing blocks is shown in Fig. 3. The output of RPB<sup>(0)</sup> and RPB<sup>(1)</sup> are produced as A, B, C and D, E, F respectively. Their sum is given to HI Detection (HID) block to detect  $x_2$ .

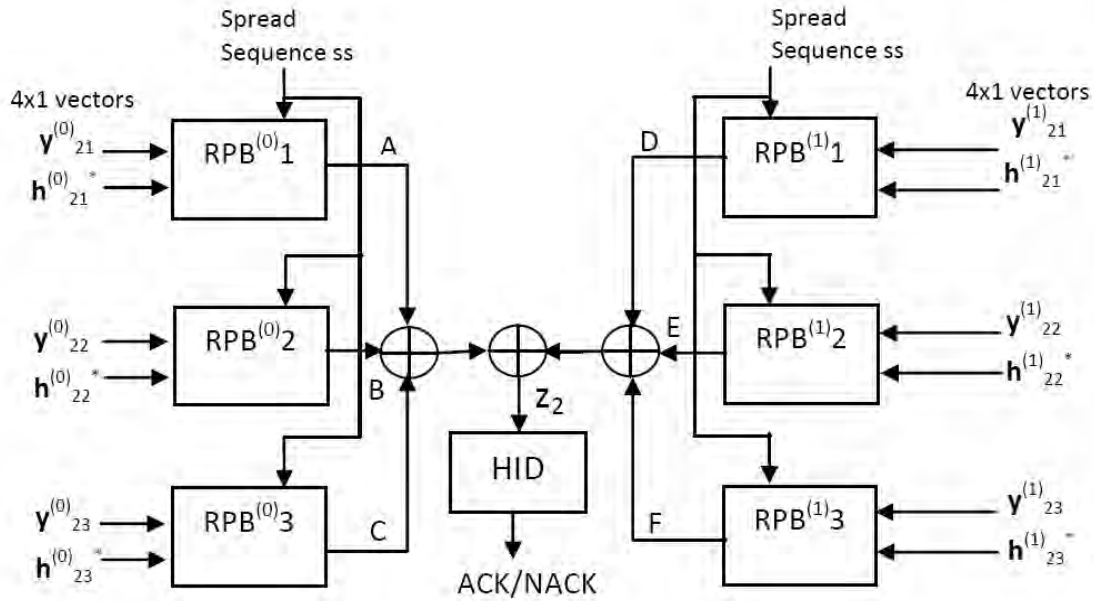


Fig. 4. Proposed SIMO 1x2 receiver architecture for PHICH.

**III.SYSTEM MODEL AND ARCHITECTURE FOR MISO AND MIMO CONFIGURATION**

In LTE-A, base station and UE have maximum of 4 and 2 antenna ports respectively, to provide transmit and receive diversities. In MISO and MIMO configurations, Alamouti’s Space Frequency Block Code (SFBC) is applied to encode two modulation symbols over two sub-carriers of the OFDM symbol [4]. In this method, the symbols  $d_0$  and  $d_1$  are encoded using the following orthogonal matrix

$$A = \begin{bmatrix} d_0 & d_1 \\ -d_1^* & d_0^* \end{bmatrix} \tag{5}$$

Matrix (5) defines the transmission format with the row index indicating the antenna number and the column index indicating the sub-carrier index. As depicted in Fig. 5, SFBC encodes a pair of symbols  $d_0$  and  $d_1$  into four variants  $d_0, d_1, -d_1^*$  and  $d_0^*$ , and transmits  $d_0$  and  $-d_1^*$ , over a certain sub-carrier from the two antennas. The symbol “\*” represents the complex conjugate of the symbol. The other two variants  $d_1$  and  $d_0^*$  are transmitted over the subsequent contiguous sub-carriers. That is, each symbol (or its conjugate) is transmitted from two antenna ports  $A_0$  and  $A_1$  and over two sub-carriers. Symbols transmitted by applying this methodology in both MISO and MIMO are received at the receiver end.

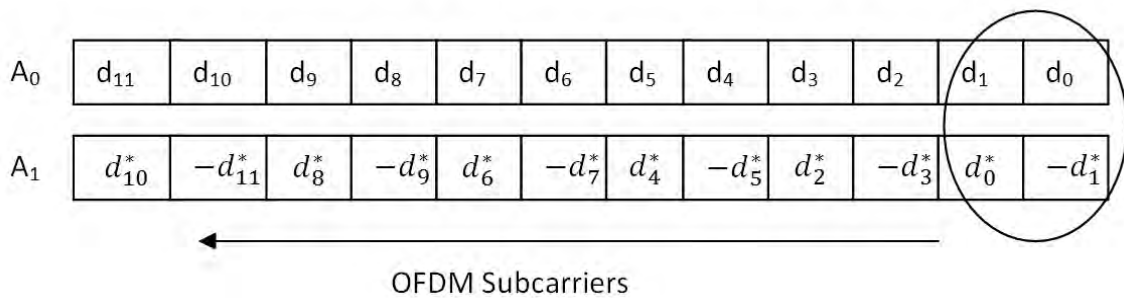


Fig. 5. Subcarrier mapping for SFBC for 2-antenna system.

For MISO 2x1, considering the signal received by the third user for  $l^{th}$  layer (two consecutive subcarriers) is given as

$$y_{3i,l} = H_{3i,l}d_{i,l} + u_{3i,l} \tag{6}$$

In (6) the value of  $l$  is considered to be 0 and 1.  $y_{3i,l}$  is a (2 x 1) received signal vector,  $d_{i,l}$  is the (2 x 1) transmit signal vector generated by layer mapping and pre-coding the HI data vector and  $u_{3i,l}$  denotes the noise vector. The channel matrix  $H_{3i,l}$  is given by

$$\mathbf{H}_{3i,l} = \begin{bmatrix} h_0 & -h_0^{(1)} \\ h_1^{(1)*} & h_1^{(0)*} \end{bmatrix} \tag{7}$$

where  $h_l^{(m)}$  is a complex channel-frequency response between  $m^{\text{th}}$  transmit antenna and the receive antenna at  $l^{\text{th}}$  symbol layer. Assuming that the channel is perfectly estimated, the maximal ratio combiner (MRC) output at the receiver is given by

$$\begin{bmatrix} z_{3i,0} \\ z_{3i,1} \end{bmatrix} = \begin{bmatrix} h_0^{(0)*} & h_1^{(1)} \\ -h_1^{(1)*} & h_1^{(0)} \end{bmatrix} \begin{bmatrix} y_{3i,0} \\ y_{3i,1} \end{bmatrix} \tag{8}$$

$$z_{3i,l} = \mathbf{H}_{3i,l}^H \mathbf{y}_{3i,l} \tag{9}$$

$\mathbf{H}_{3i,l}^H$  denotes the conjugate transpose of  $\mathbf{H}_{3i,l}$ . By ML decision rule, the decision statistic  $z_3$  is given by

$$z_3 = \sum_{i=1}^3 \text{Re} \left\{ \sum_{l=0}^1 \langle z_{3i,l}, \mathbf{w}_3 \rangle \right\} \tag{10}$$

where  $z_{3i,l}$  is the  $l^{\text{th}}$  (4x1) vector with  $z_{31,l}=[z_{3,0}, z_{3,1}, z_{3,2}, z_{3,3}]$ ,  $z_{32,l}=[z_{3,4}, z_{3,5}, z_{3,6}, z_{3,7}]$ ,  $z_{33,l}=[z_{3,8}, z_{3,9}, z_{3,10}, z_{3,11}]$ . For MISO (2 x 1) architecture, a mix of two signals from two antennas with different channel estimations and noise is received at the receiver as shown in Fig. 6. It has three receiver processing blocks (MISO RPB- $i$ ) where  $i=1, 2, 3$  and a HI detection (HID) block.

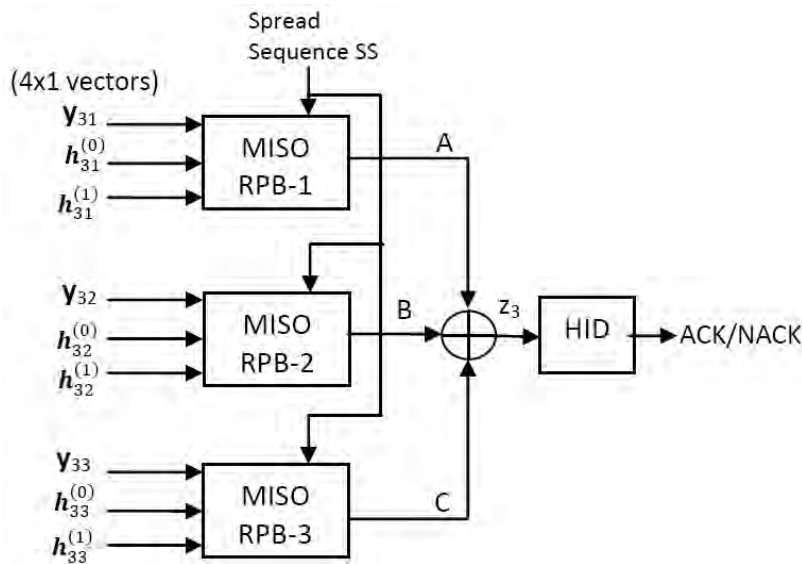


Fig. 6. Proposed MISO 2x1 receiver architecture for PHICH

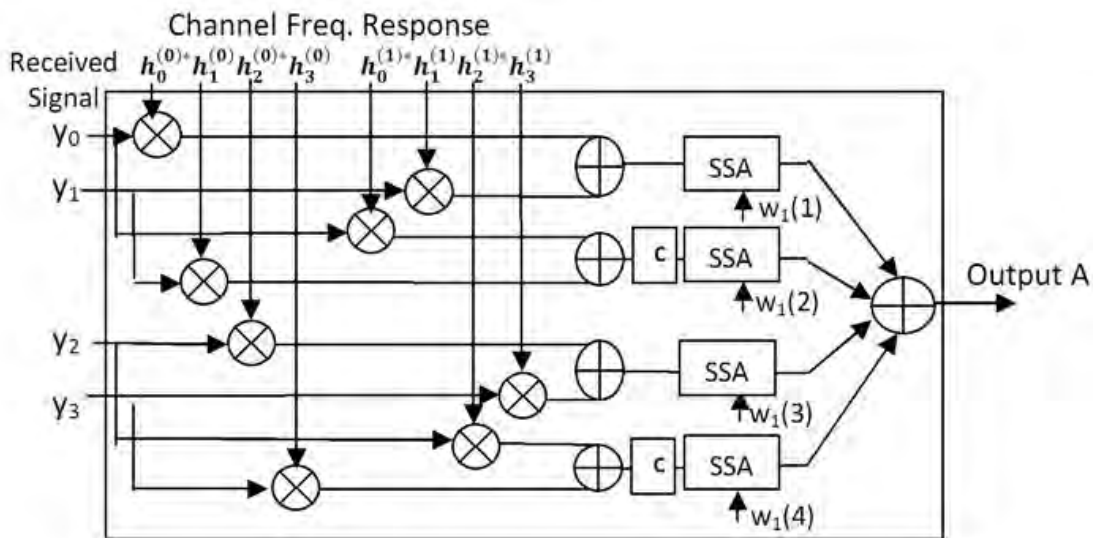


Fig. 7. Internal architecture of MISO Receiver Processing Block (MISO RPB-1)

The internal structure of MISO RPB-1 is shown in Fig. 7. The received signals from two antennas are multiplied with the channel estimation matrix. The block ‘c’ refers to the conjugate operation processed for the even pair according to (8). The result is fed to SSA and added together to get the output A. The number of complex multiplications is 8 for one MISO RPB. Similar operations are carried out in MISO RPB-2 and MISO RPB-3 to get the decoded output value B and C. Sum of A, B and C is given to HID block to detect  $x_3$ .

MIMO systems have emerged as an attractive technique for achieving efficient transmission data rate and bandwidth [5]. In MIMO system, the received signals of UE-4 at  $l^{th}$  layer (two consecutive subcarriers), for  $k^{th}$  receive antenna is given by

$$\mathbf{y}_{4i,l}^{(k)} = \mathbf{H}_{4i,l}^{(k)} \mathbf{d}_{i,l} + \mathbf{u}_{4i,l}^{(k)} \tag{11}$$

$\mathbf{y}_{4i,l}^{(k)}$  is the (4x1) received signal vector,  $\mathbf{d}_{i,l}$  is (2 × 1) transmit-signal vector, and  $\mathbf{u}_{4i,l}^{(k)}$  denotes (4 × 1) noise vector. The channel matrix

$$\mathbf{H}_{4i,l}^{(k)} = \begin{bmatrix} h_l^{(0,0)} & h_l^{(0,1)} \\ h_l^{(1,0)} & h_l^{(1,1)} \\ h_l^{*(0,1)} & -h_l^{*(0,0)} \\ h_l^{*(1,1)} & -h_l^{*(1,0)} \end{bmatrix} \tag{12}$$

where  $h_l^{(k,m)}$  is a complex channel-frequency response between  $m^{th}$  transmit antenna and  $k^{th}$  receive antenna at  $l^{th}$  symbol layer [6], [7]. The maximal ratio combiner (MRC) output at the MIMO receiver is given by

$$\mathbf{z}_{4i,l}^{(k)} = \mathbf{H}_{4i,l}^{(k)H} \mathbf{y}_{4i,l}^{(k)} \tag{13}$$

where  $\mathbf{H}_{4i,l}^{(k)H}$  denotes the conjugate transpose of  $\mathbf{H}_{4i,l}^{(k)}$ . By ML decision rule, the decision statistic  $z_4$  is given by

$$z_4 = \sum_{i=1}^3 \sum_{k=0}^K Re \left\{ \sum_{l=0}^1 \langle \mathbf{z}_{4i,l}^{(k)}, \mathbf{w}_4 \rangle \right\} \tag{14}$$

where  $\mathbf{z}_{4i,l}^{(k)}$  is the  $i^{th}$  (4x1) vector with  $\mathbf{z}_{41,l}^{(k)} = [z_{4,0}^{(k)}, z_{4,1}^{(k)}, z_{4,2}^{(k)}, z_{4,3}^{(k)}]$ ,  $\mathbf{z}_{42,l}^{(k)} = [z_{4,4}^{(k)}, z_{4,5}^{(k)}, z_{4,6}^{(k)}, z_{4,7}^{(k)}]$ ,  $\mathbf{z}_{43,l}^{(k)} = [z_{4,8}^{(k)}, z_{4,9}^{(k)}, z_{4,10}^{(k)}, z_{4,11}^{(k)}]$ .

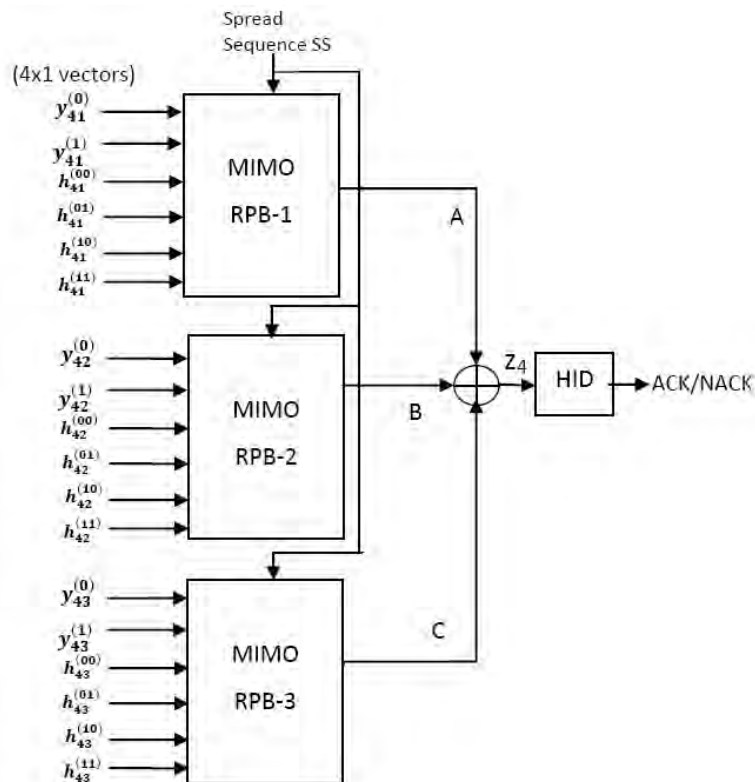


Fig. 8. Proposed MIMO 2x1 receiver architecture for PHICH.

MIMO 2x2 architecture shown in Fig. 8 is similar to MISO architecture but the receiver has two receiving antennas and hence for each receiving antenna a mix of two signals from two transmitting antennas with different channel estimations and noise is received. The architecture has three receiver processing blocks (MIMO-RPB) and their output is fed to HID block. The internal structure of MIMO RPB-1 is as shown in Fig. 9. The received signal from two antennas is multiplied with the transpose conjugate of the channel matrix. The result is fed to SSA and added together to get the decoded output A. The number of complex multiplications is 16 for one MIMO-RPB. Similar operations are carried in MIMO-RPB 2 and MIMO-RPB 3 to get the decoded outputs B and C. A, B and C are added and given to HID block to detect  $x_d$ .

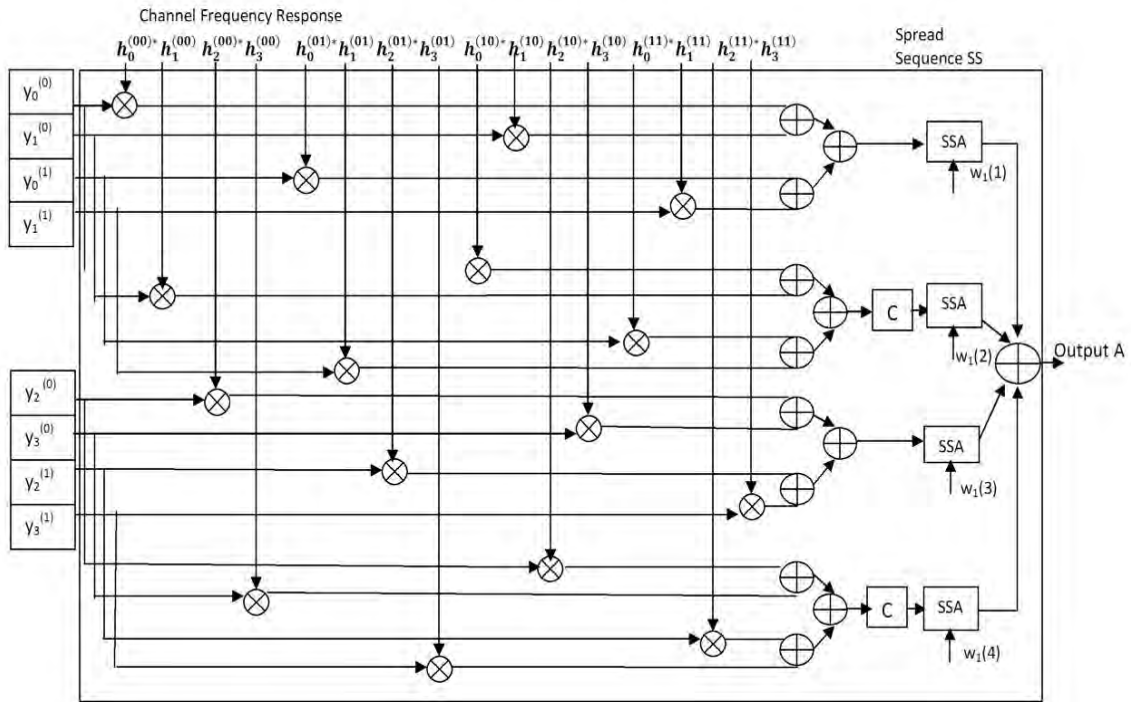


Fig. 9. Internal architecture of MIMO Receiver Processing Block (MIMO-RPB-1).

#### IV. IMPLEMENTATION METHODS

##### A. Direct Implementation with Multiplicands Rearranged Method

In all the RPBs complex multiplications are involved due to the multiplication of  $H^H$  matrix with the received signal. Hence, there is increase in the number of multiplications in the entire estimation process. The number of multiplications utilized in the implementation is reduced by rearranging [4]. The intermediate products are reused in real and imaginary part calculation. Consider the multiplication of two complex numbers  $\text{Re}\{h\} + j \text{Im}\{h\}$  and  $\text{Re}\{y\} + j \text{Im}\{y\}$ . The output real part ( $e$ ) and imaginary part ( $f$ ) terms are given by

$$e = \text{Re}\{h\} \times \text{Re}\{y\} - \text{Im}\{h\} \times \text{Im}\{y\} \tag{15}$$

$$f = \text{Re}\{h\} \times \text{Im}\{y\} + \text{Im}\{h\} \times \text{Re}\{y\} \tag{16}$$

It requires four multiplications and two additions. The terms in (15) and (16) can be rearranged as

$$e = [\text{Re}\{y\} - \text{Im}\{y\}][\text{Re}\{h\} - \text{Im}\{h\}] - \text{Re}\{y\} \text{Im}\{h\} + \text{Im}\{y\} \text{Re}\{h\} \tag{17}$$

$$f = \text{Re}\{y\} \text{Im}\{h\} + \text{Im}\{y\} \text{Re}\{h\} \tag{18}$$



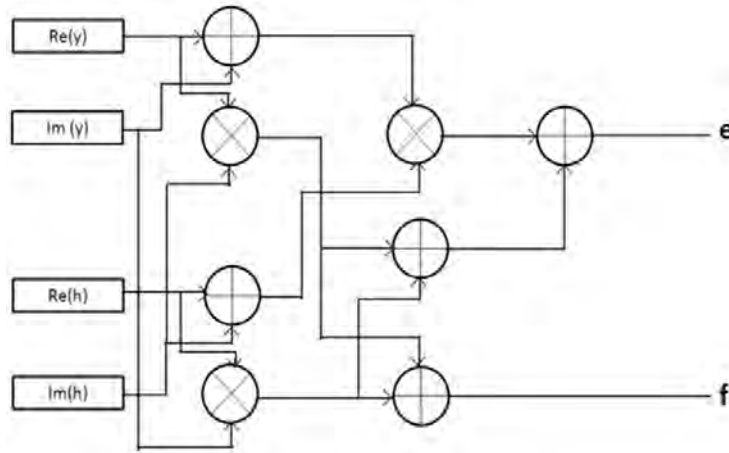


Fig. 10. Multiplicands rearrangement for a single complex multiplication block

It requires only three multiplications but five additions, because the terms  $Re\{y\}Im\{h\}$  and  $Im\{y\}Re\{h\}$  are repeated in both the equations. This rearrangement of multiplications is employed in the decoding part of the architecture at the cost of increased additions as shown in Fig. 10.

**B. Folding Architecture**

Considering the limited availability of multipliers in Virtex 5 FPGA device, folding is introduced to restructure the system into several levels of logic and breaking them up over multiple clocks such that multiple operations are time multiplexed to a single functional unit. For PHICH, the 12 received subcarriers are stored in register and the first 4 subcarriers involve in computation to get the value A. The same hardware is then utilized by the remaining subcarriers in the subsequent clock cycles to get the values B and C.

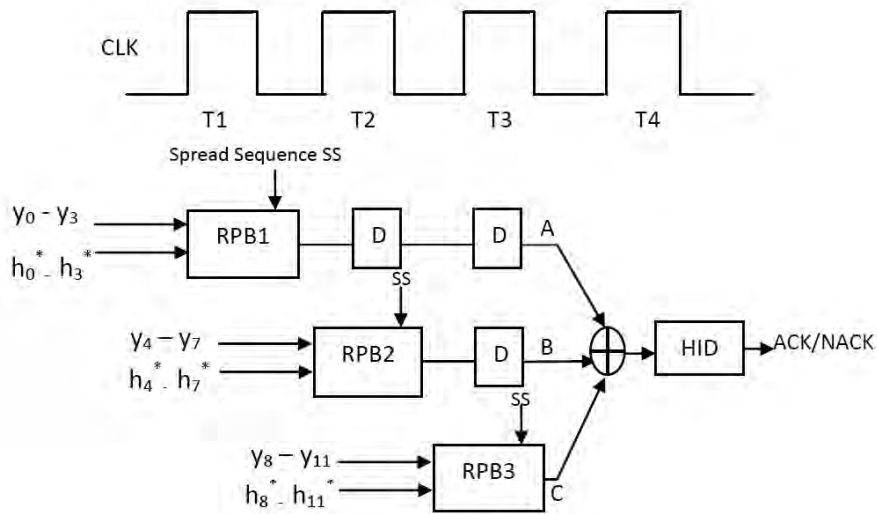


Fig. 11. Folding architecture for SISO considering one RPB per clock cycle.

Fig. 11 shows the folding architecture for SISO where same hardware (RPB) is utilised by RPB1, RPB2 and RPB3. Similarly in SIMO,  $RPB^{(0)}$  and  $RPB^{(1)}$  are pipelined and in MISO and MIMO corresponding MISO-RPB and MIMO-RPB are pipelined. The internal folding architecture for an RPB is shown in Fig. 12. The same hardware is used for all RPBs. Further variation of resource utilisation in this architecture, varies the timing for the completion of the operation as shown in Table III.

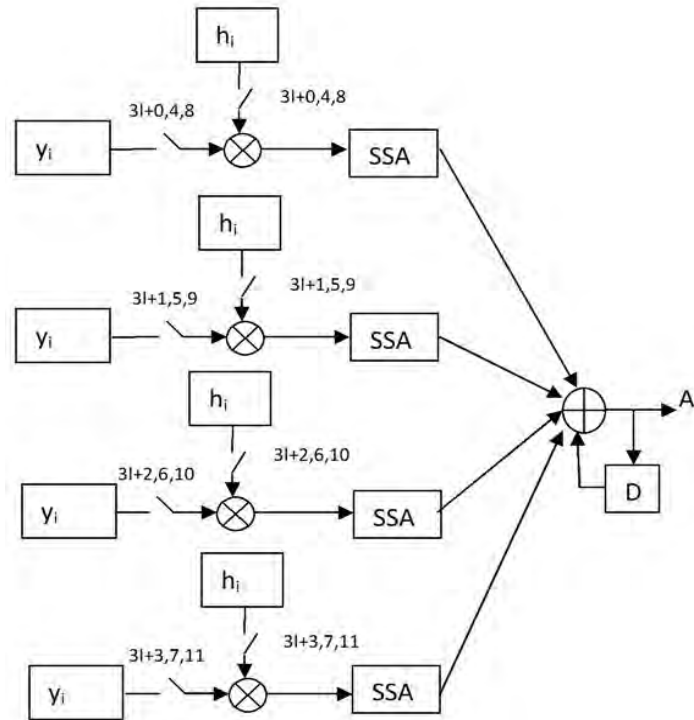


Fig. 12. Internal folding architecture for RPB.

As the resource elements per clock cycle are reduced, the total number of clock cycles to complete the entire operation would increase and also lead to increase in complexity as it requires more registers to store and accumulate the values before final decisional step. There is a trade off between time units, operational resources and the register requirements. Hence 4 clock cycle configuration is considered as a better option.

TABLE III  
Reduced multiplications and increase in delay for folding method.

S.No	Number of Multiplications			Total number of clock cycles
	SISO	SIMO/MISO	MIMO	
1.	12	24	48	4
2.	6	12	24	7
3.	3	6	12	13

C. Parallel Processing with Folding Architecture

In this method, the hardware resources are utilized simultaneously in all the RPBs as shown in Fig. 13 for SISO configuration. There are four hardware lines in each RPB. Only one hardware line from each RPB is used per clock cycle. Similarly in SIMO one hardware line each from RPB<sup>(0)</sup>-1,2,3 and RPB<sup>(1)</sup>-1,2,3 is considered in each clock cycle and in MISO and MIMO one hardware line at a time from corresponding MISO-RPB-1,2,3 and MIMO-RPB-1,2,3 are computed per clock cycle. This method requires 5 clock cycles to compute a set of 9 multiplications for SISO, 18 for SIMO/MISO and 36 for MIMO requiring less hardware resources, at the cost of increase in one clock cycle compared to normal folding method.

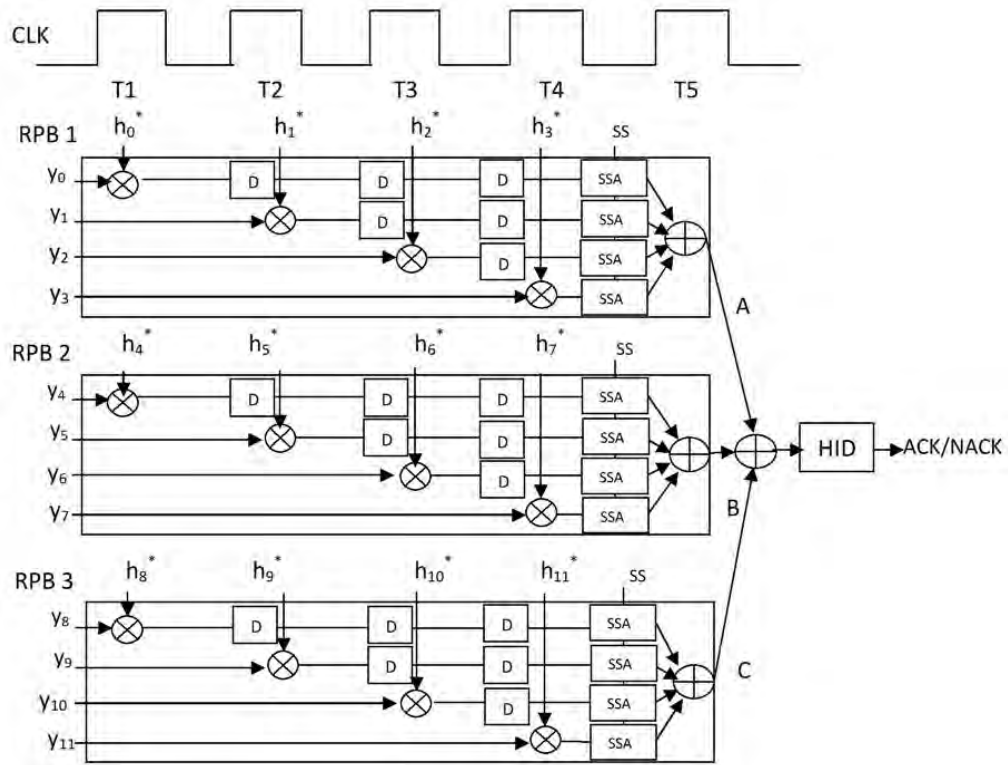


Fig. 13. Parallel processing with folding architecture for SISO considering one hardware line for each RPB per clock cycle.

**V. SIMULATION AND SYNTHESIS RESULTS**

The receiver architecture is synthesised using the Xilinx PlanAhead tool on the Virtex-5 FPGA-xc5vlx50tff1136-1 device. Table IV shows the performance of direct multiplication rearranged (MR), folding method (for 4 clock cycles) and parallel processing with folding architecture (for 5 clock cycles) in terms of resource utilisation, speed and power for SISO, 1 x 2 SIMO, 2 x 1 MISO and 2 x 2 MIMO configurations.

TABLE IV  
Comparison table for direct, folding and parallel processing with folding methods

Diversity	Method	Multipliers	Adders	Max Delay (ns) in one clock cycle (1T)	Speed (MHz)	Power (mW)
SISO	Direct MR	38	106	2.247	445.038	443
	Folding(4T)	14	38	2.500	400.000	529
	Parallel with folding(5T)	11	62	2.247	445.038	560
SIMO	Direct MR	74	211	2.505	399.202	443
	Folding(4T)	26	78	1.987	503.271	625
	Parallel with folding(5T)	20	122	2.247	445.038	684
MISO	Direct MR	74	202	2.527	395.726	443
	Folding(4T)	26	74	2.527	395.726	640
	Parallel with folding(5T)	20	92	2.527	395.726	696
MIMO	Direct MR	146	478	2.527	395.726	443
	Folding(4T)	50	162	2.527	395.726	1022
	Parallel with folding(5T)	38	155	2.527	395.726	1156

In all these methods multiplication rearrangement is employed. The resource elements like multipliers and adders increase for the SIMO, MISO and MIMO environment. When direct method is implemented, only static power exists. Hence the power consumption is less when compared to folding and parallel processing methods

which also include dynamic power. The frequency of operation is same in MISO and MIMO for all methods. Parallel processing with folding is found to be the best architecture for PHICH as it uses less resource with better speed of operation and medium power consumption. Using this method a single architecture synthesized considering all diversity environments. Synthesis of the single architecture displays low resource utilization.

Fig. 14 shows the simulation waveform for the overall architecture including all diversities. The input variable 'diversity' is used to select the antenna configuration from the binary values '00' for SISO, '01' for SIMO, '10' for MISO and '11' for MIMO. This enables or disables the control variable 'en' to the corresponding modules. Output registers 'count\_ACK' and 'count\_NACK' accumulate the number of acknowledgements and negative acknowledgements respectively detected at the receiver for the selected diversity. Variables 'ack1' to 'ack8' denote the HARQ Indicator (HI) values of 8 UEs that are processed and transmitted to the receiver. In the waveform when diversity is '00', control variable 'e' enables the SISO module through 'div0/en'. Considering UE-4 to be the receiver, ack4 is detected to be '1' and hence corresponding register 'count\_ACK1' increases by 1 (at 1500ps). At 2000ps count\_NACK1 is incremented after detecting a NACK in SISO mode. When diversity is set to '01', SIMO module is enabled by 'div1/en' disabling the other 3 diversities. Consequently register 'count\_ACK2' incremented when ACK is detected. Similar operations are carried out in MISO and MIMO modules.

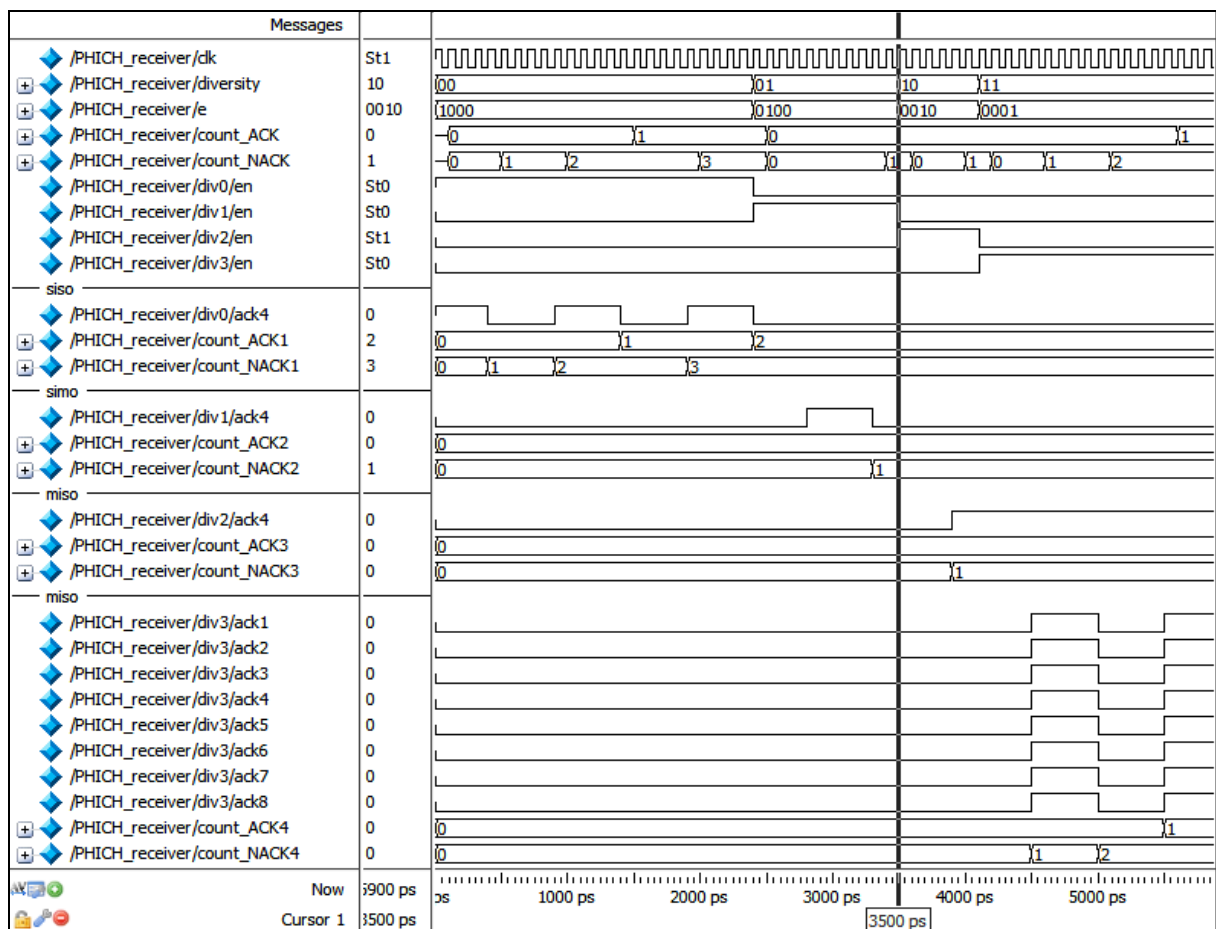


Fig. 14. Simulation waveform for PHICH receiver.

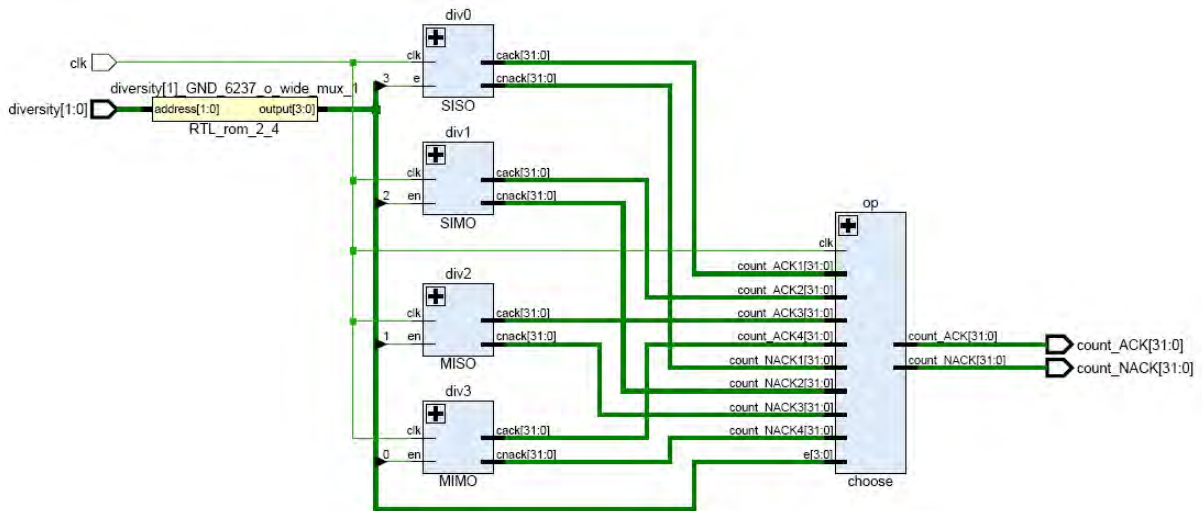


Fig. 15. RTL Schematic of a single architecture using parallel processing with folding method considering all the diversity modules.

The RTL schematic is shown in Fig. 15 shows the different modules. Fig.16 shows the image of FPGA editor for the PHICH receiver architecture. Around 632 slices, 778 registers and 24 DSP48E components are used for the total architecture of PHICH in xc5vlx50tff1136-1 device. The resource utilization, frequency of operation and power consumption of the single architecture is shown in Table V. The delay involved in detecting the HARQ Indicator meets the 1.068  $\mu$ s constraint.

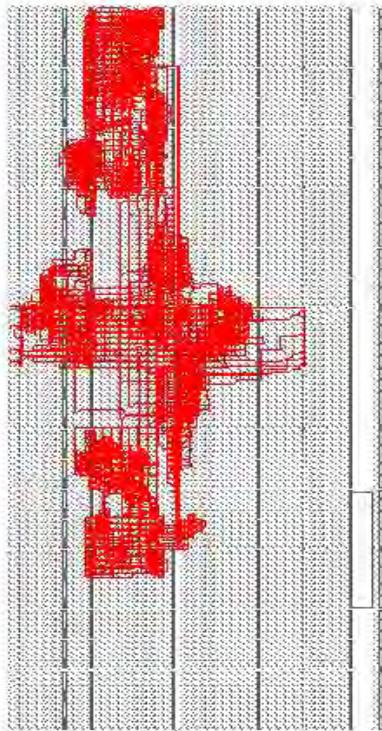


Fig. 16. Implemented device in FPGA editor for PHICH receiver architecture.

TABLE V  
PHICH receiver architecture with diversity.

Multipliers	Adders	Max Delay (ns) for one Time cycle (1 T)	Total Max Delay (ns) (5 T)	Speed (MHz)	Power (mW)
89	439	2.824	14.12	70.821	1475

## VI. CONCLUSION

In this paper a low complexity, low resource single or multi-antenna detection at the receiver system has been proposed and analyzed using Modelsim and implementation in the Virtex 5 device in Xilinx PlanAhead tool. In the detector, computational complexity and the resource utilized are minimized by employing arithmetic operational rearrangement and sub optimal sequential DSP algorithm called the folding approach along with parallelism. The proposed system is compared in terms of different folding and parallel configurations adopted in the system with tradeoff between the timing cycles, operational resources and the complexity in manipulation involved in the HARQ Indicator detection. The results show that the proposed system that employs parallel processing with folded approach is optimal compared to other possible ways, also meeting the LTE frame timing constraint. The proposed system is a suitable solution for the area optimized hardware implementation of receiver structures for PHICH, the LTE-A physical downlink control channel.

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