Digital Filter Architectures for Multi-Standard Wireless Transceivers

R.Latha[#1], P.T.Vanathi[*2]

[#]Electronics & Communication Engineering Department, Christ University-Faculty of Engineering, Bangalore-560 060, Karnataka, India.
lathagopal26@gmail.com

[*]Electronics & Communication Engineering Department, P.S.G. College of Technology, Coimbatore- 641 004, Tamilnadu, India.
ptvani@yahoo.com

Abstract— This paper addresses on two different architectures of digital decimation filter design of a multi-standard RF transceivers. Instead of using single stage decimation filter network, the filters are implemented in multiple stages using FPGA to optimize the area and power. The proposed decimation filter architectures reflect the considerable reduction in area & power consumption without degradation of performance. The filter coefficients are derived from MATLAB , the filter architectures are implemented and tested using Xilinx SPARTAN FPGA . The Xilinx ISE 9.2i tool is used for logic synthesis and the Xpower analysis tool is used for estimating the power consumption. First, the types of decimation filter architectures are tested and implemented using conventional binary number system. Then the different encoding scheme i.e. Canonic Signed Digit (CSD) representation is used for filter coefficients and then the architecture performance is tested .The results of CSD based architecture shows a considerable reduction in the area & power against the conventional number system based filter design implementation.

Keywords-Digital Filter, Decimation Filter, FPGA, Hardware Reduction, Low Power Design.

I. INTRODUCTION

Current research on Radio Frequency (RF) communication transceivers emphasizes both higher integration to meet consumer demand of low-cost, low-power, less area personal communication devices and the ability to adapt to Multiple Communication Standards. Higher integration can be achieved by using receiver architectures and circuit techniques that eliminate the need for external components. Receiver architecture that performs channel select filtering based on-chip at baseband allows for the programmability necessary to adapt to Multiple Communication Standards[1]. In audio applications of wireless transceivers, the use of oversampling Sigma Delta Analog to Digital (∑Δ-ADC) converter has become popular because of its improved performances and flexibility. Consider an analog input signal with maximum frequency of f_x, which is sampled by the oversampling Sigma Delta Analog to Digital converter[2]. The ∑Δ-ADC converter samples the input signal with rate much greater than Nyquist rate $2f_x$.The oversampling ratio of the ∑Δ-ADC is defined as $M = f_s/2f_x$,where f_s is the sampling rate of ∑Δ-ADC converter and $2f_x$ is the Nyquist rate. Typical audio application consists of an oversampled ∑Δ-ADC followed by a decimation filter. The digital decimation filter is used to perform filtering operation and sampling rate down conversion so as to extract the original signal bandwidth or the band of interest from the oversampled ∑Δ-ADC. A programmable low-pass digital decimation filter of a RF transceiver can select a desired channel in the presence of both strong adjacent channel interference and quantization noise from the digitizing process.

Several literatures deal with the design issues of decimation filters for wireless communication transceivers. In this paper, a cascade CIC–HB filter implementation of the decimation filter using Conventional and CSD based multipliers are addressed in detail. This paper is organized as follows: Section 2 describes the digital receiver architecture suitable for multi-standard operation. Section 3 deals with the concepts of decimation process. Section 4 presents the two different multistage decimation filter architectures and types of filters used for implementation of each stage. In Section 5 Canonic Signed Digit (CSD) representation is explained in detail[3]. Section 6 provides the simulation results of the various types of decimation filter architectures. Finally Section 7 describes the conclusion and future work.

II. DIGITAL RECEIVER ARCHITECTURE

This section deals with the digital receiver architecture, which emphasizes high integration and multi-standard capability. High integration can be achieved by utilizing a receiver architecture that performs base band channel select filtering on-chip. This enhances the programmability to different dynamic range, linearity and signal bandwidth so as to meet the requirements of multiple RF standards. Typical block diagram of a digital transceiver is shown in Fig.1. An overview of a digital receiver will readily confirm that its main task is to take a signal sampled at a high rate, down convert it and filter it-through low-pass filter and then decimate it and

finally format it into one or more of several forms. After demodulation, this signal is converted back to analog form and then applied to power amplifier and loudspeaker.

The input analog signal is converted to digital form with the aid of the A/D converter. A wide band, high dynamic range sigma-delta modulator can be used to digitize both the desired signal and potentially stronger adjacent channel interferences. Next, this signal compromising of ones and zeros is applied to a digital Mixer, just as in the case of analog receiver. Only at this time, the signal is applied to two Mixers driven by digital In-phase (I) and Quadrature (Q) components of a local oscillator signal which in turn is provided by a digital frequency synthesizer. In essence, the input signal is multiplied with the sine and also with the cosine output of the local oscillator. Just as in the case of the analog receiver, the output of the Mixer consists of sum and difference frequencies extending the way up in the sampled data spectrum. To remove the higher order components and to recover only the baseband signal, the signal is passed through a Decimating Low Pass Filter. This digital filter has the property of reducing the sample rate of the input signal by some factor(decimation factor) , which can be programmed to be as low as 1 or as high as 16,384.The filter output signal is formatted and this is made available in one or more of several forms. As far as the demodulator function is concerned, it is best performed digitally in a DSP processor outside the digital receiver chip. Demodulator is followed by a D/A converter and speaker to complete the analogy between the analog and digital receivers.

III. NEED FOR DECIMATION PROCESS

To reconstruct a signal from its sample values, a band-limited signal only need to be sampled at a rate in excess of the Nyquist rate. Speech or low bandwidth signals may be sampled well above their Nyquist rate to bypass problems associated with the low rate analog to digital conversion. This is achieved using Sigma Delta A/D converter(ΣΔ- ADCs) in the digital receivers. One of the key features of Sigma Delta A/D converter is that the modulator is over sampled compared to the expected output sample rate. Decimation is an important component of over sampled analog to digital conversion (ΣΔ- ADCs). A higher order decimation filter is used to convert the over sampled signal into usable baseband signal. The decimation process simply reduces the output sample rate while retaining the necessary information. It transforms the digitally modulated signal from short words occurring at high sampling rate to longer words at Nyquist rate. To extract the signal information, the signal must be first down-converted to base band. A multi-stage decimation filter is used to perform this function.

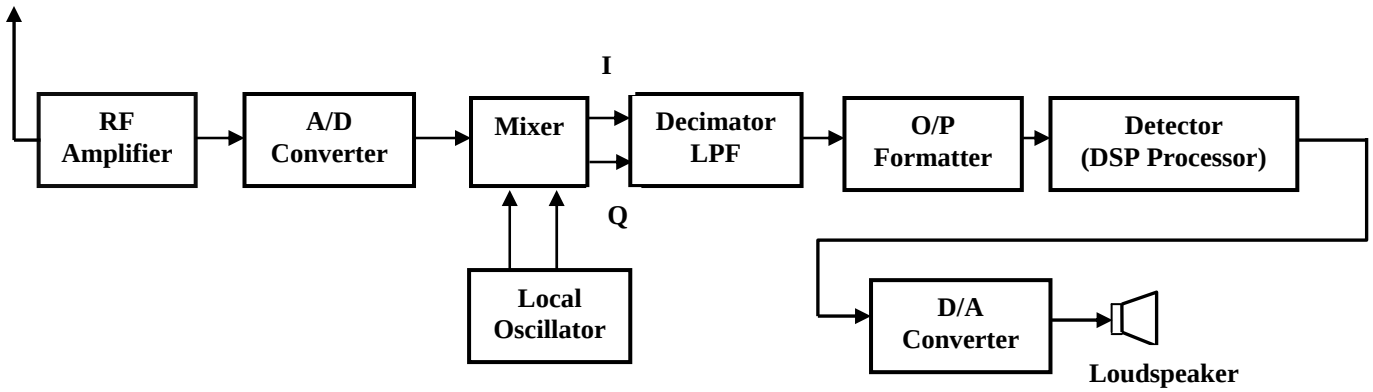

Fig. 1. Architecture of Digital Transceiver

As far as initial stage of decimation is concerned, the word rate decreases to about four times the Nyquist rate. In all these cases, high decimation rates are required to reduce the output bandwidth which can be processed with conventional hardware. Due to over sampled ΣΔ- ADCs , only small fraction of the total noise power falls in the frequency band of interest which is shown as quantization noise power spectral component in Fig.2.

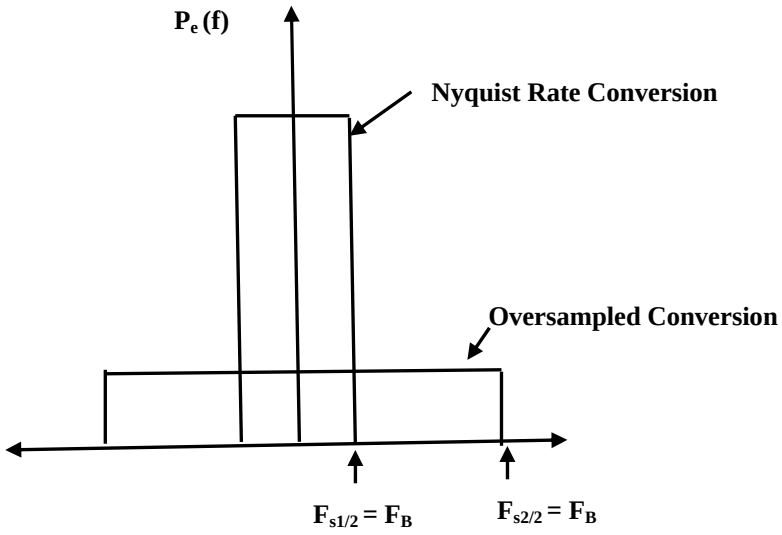

Fig. 2. Quantization Noise Power Spectral Densities of A/D Converters

The noise power outside the signal band can be greatly attenuated with a digital low pass decimation filter following the ΣΔ- ADC. Decimation is often performed in several stages instead of a single stage. This leads to higher decimation factor in the first filter stage as compared with decimation filters of similar input and output data word lengths in the consecutive stages. However, the word length differs between the consecutive stages. This is especially important for ΣΔ ADCs, as the input to the decimator may be only one bit while the output precision can be, say, 16 bits or more. Multistage decimation filter architecture reduces the overall complexity in terms of area and power at each stage of filter design.

IV. MULTISTAGE DECIMATION FILTER ARCHITECTURES

The sampling rate is down converted from the oversampled rate of sigma-delta modulator to a data rate that can be conveniently processed by existing DSP processors using decimation filters. This minimizes the power consumption of DSP processors for demodulation and equalization. The purpose of decimation filter is to remove all the out-of-band signals and noise and to reduce the sampling rate from oversampled frequency of the ΣΔ- ADC to Nyquist rate of the channel[5]. The decimation filter consists of a low-pass filter and a down-sampler. It is possible to perform noise removal and down conversion with a single FIR filter stage. The filter order N of FIR low-pass filter is given by eqn. (1), where D_∞ is a function of the required ripples δ_p and δ_s in the pass-band and stop-band respectively, F_s is the sampling frequency and Δf is the width of transition band.

$$N \approx D_\infty(\delta_p, \delta_s)(F_S/\Delta f) \quad (1)$$

As the ΣΔ- ADCs are oversampled, the transition band is small relative to the sampling frequency leading to excessively large filter orders and this leads to a lot of multiplication operations. The power consumption of the filter depends on the number of taps as well as the rate at which it operates. So computational complexity is high for single stage implementation of decimation filter and consumes more power. Implementing decimation filter in several stages reduces the total number of filter coefficients. Subsequently, the hardware complexity and computational effort are reduced in multistage approach. This will result in less area and low power consumption. A multistage decimation filter system consists of a cascaded structure of several single stage decimation filter systems. The 'i^{th}' stage of multistage system performs decimation by a factor of 'R_i' such that the overall decimation factor 'R' is given by the eqn. (2)

$$R = \Pi(R_i) \ , where\ i = 1,2,3 \ldots . P \quad (2)$$

where 'P' is the total number of stages of multistage decimation filters. The individual filter of each stage is designed within the frequency band of interest in order to prevent aliasing in the overall decimation process. The performance of a decimation filter depends on the filter architecture and the order of each stage of a multistage decimator. FIR filters are widely used in decimators because of its linear phase characteristics. Multiple contributions are proposed in previous works for multi-standard multi stage digital filters for decimation and channel selection. Multistage decimation reduces the overall complexity of system by decomposing the decimation factor into several sub factors. Thus, each stage requires lower order filters. Moreover, after four to five stages, the filter complexity is not further reduced. Therefore, a trade off between the number of stages and complexity must be achieved.

FIR filter are used in down converters because some modulation schemes requires linear phase. In wireless communication devices, the battery life must be maximized. Therefore, high performance blocks with low power consumption and small area are required. The implementation of decimation filter for multiple standards on a single device is very demanding in terms of area and power. With an efficient decomposition of decimation factor considering common blocks between different communication standards, it is possible to have an efficient design. Thus, few different blocks could be implemented in a configurable fashion.The two different filter architectures of this paper are described in the following sections in detail.

A. Architecture I:

Decimation Filter with Conventional MAC Unit

In this architecture, decimation filter is implemented using two filter stages with a overall decimation factor of 32. The decimation filter architecture consists of first stage representing High Order Decimation Filter (HDF) and second stage representing corrector Finite Impulse Response (FIR) filter and implemented using conventional binary number system with conventional MAC unit as shown in fig.3.

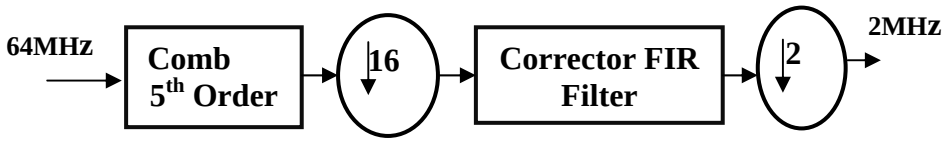

Fig. 3. Two Stage Decimation Filter with Conventional MAC Unit

1) Cascaded Integrator Comb(CIC) Filter:

The first filter section is called the HDF and it is normally optimized to perform decimation by large factors. It implements a low pass filter function using only adders and delay elements instead of a large number of multiplier/accumulators that would be required using a standard FIR filter. An efficient architecture of HDF stage belongs to a class of multi-rate multiplier-less systems referred to as Cascade of Integrators-Comb (CIC) filters[4]. In fact, in its recursive form, the CIC filter is multiplier less and presents low complexity properties. The fifth order CIC filter structure is shown in fig.4. It is constructed using only integrators and differentiators. Blocks I represent the integrators, R represents the decimator and D represent the differentiators (comb).The CIC filter design approach consists of 5 stages of Integrator section followed by a 5 stages of differentiators. The cascaded structure of integrators and combs provides a better solution for low power CIC filters.

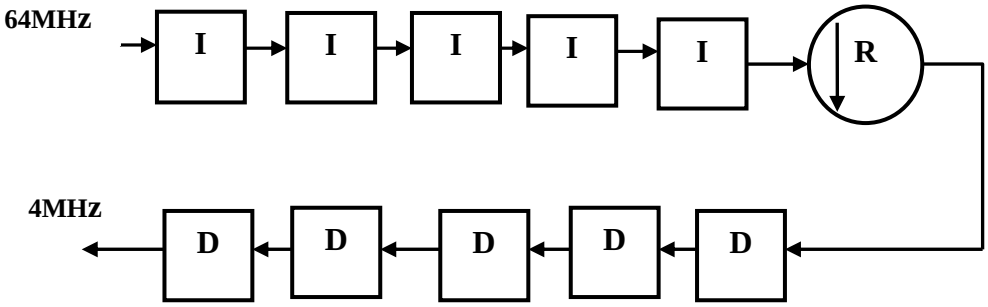

Fig. 4. Fifth Order CIC Filter Structure

The integrator (I) and the comb filter (D) operations are performed using registers and adders only. Fig.5 shows the equivalent digital circuit representation of the integrator stages. Each accumulator is implemented as an adder followed by a register in the feed forward path. The integrator is clocked by the sample clock, CK_IN as shown in Fig. 5. The output of the Integrator section is latched on to the decimation register by CK_DEC. The output of the decimation register is passed to the Comb Filter Section. The Comb section consists of five cascaded comb filters. Each Comb filter section calculates the difference between the current and previous integrator output. Each comb filter consists of a register which is clocked by CK_DEC followed by an subtracter where the subtracter calculates the difference between the input and output of the register. Fig.6 describes the equivalent digital circuit representation of the 5- stage comb filter.

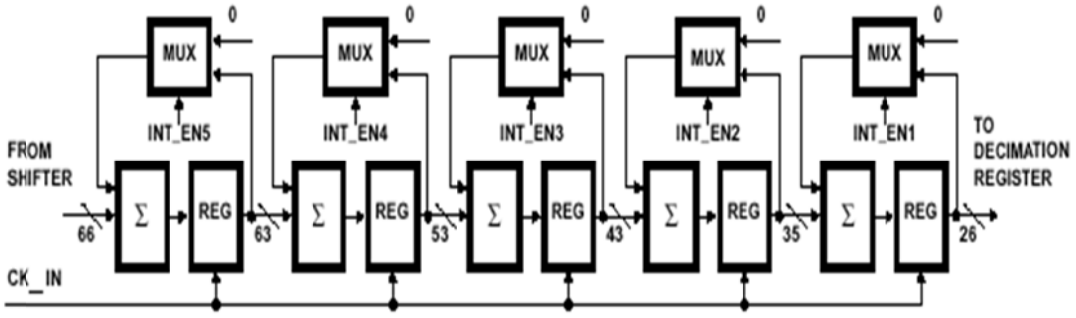

Fig. 5. Digital Circuit Implementation of 5-Stage Integrator

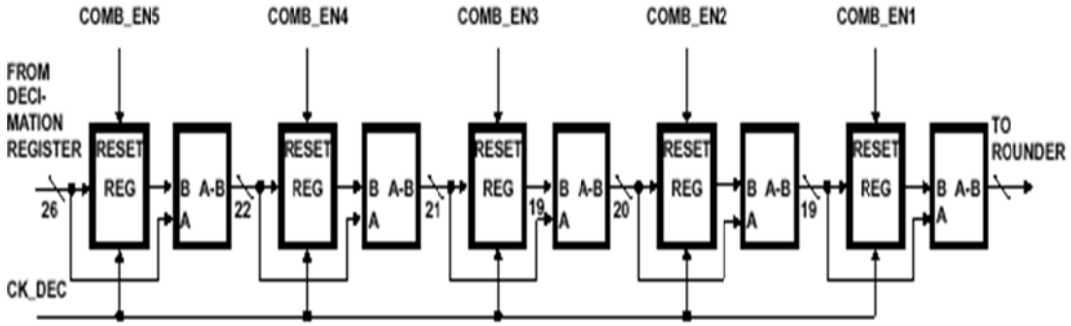

Fig. 6. Digital Circuit Implementation of 5-Stage Comb Filter Section

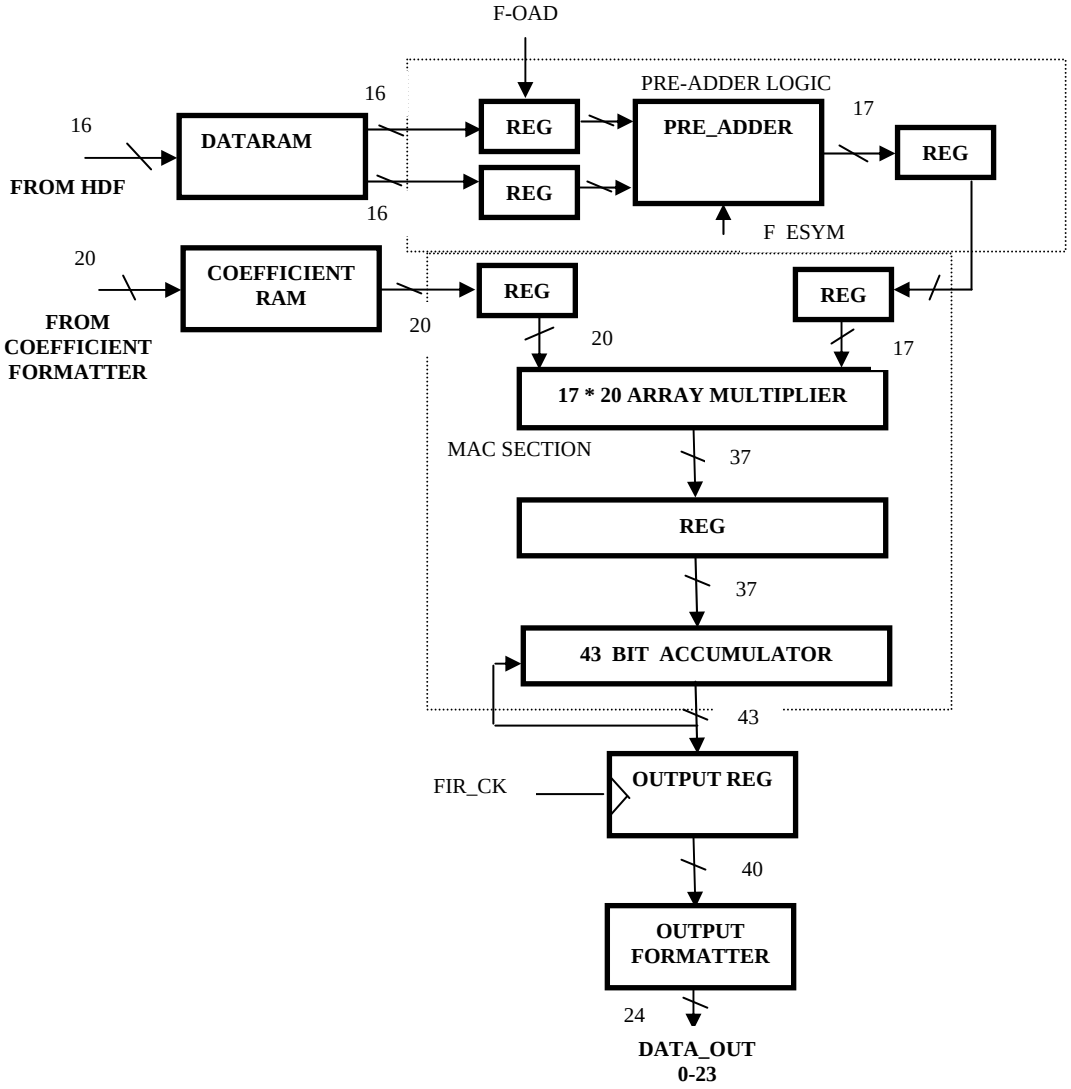

Fig. 7. Corrector FIR Filter using MAC Unit

2) Characteristics of CIC filter:

The integrator section of CIC filter consists of N ideal digital integrator stages operating at high sampling rate, f_s. Each stage is implemented as a one-pole filter with a unity feedback coefficient. The system function for a single integrator is given by eqn. (3).

$$H_1\ (Z) = \frac{1}{1-Z^{-1}} \tag{3}$$

The comb section operates at the low sampling rate f_s/R, where R is the integer rate change factor. This section consists of N comb stages with a differential delay of M samples per stage. The differential delay is a filter design parameter used to control the filter's frequency response. In practice, the differential delay is usually held at M = 1 or 2. The system function for a single comb stage referenced to high sampling rate is denoted by eqn. (4).

$$H_C\ (Z) = (1 - Z^{-RM}) \tag{4}$$

Where R = Decimation ratio

M =Differential delay

N = No. of stages

It follows from eqn. 3 and eqn. 4 that the system function for the composite Nth order CIC filter referenced to the high sampling rate, fs is denoted by eqn. 5 as

$$H(Z) = H_1^N(Z) \times H_C^N(Z) = (1 - Z^{-RM})^N/(1 - Z^{-1})^N$$
$$= [\sum Z^{-k}]^N \tag{5}$$

where k ranges from 0 to RM-1

It is implicit from the last form of the system function that the CIC -HDF filter is functionally equivalent to a cascade of N uniform FIR filter stages[8].

3) Corrector FIR Filter:

The second filter stage in the top level block diagram of architecture I is a corrector Finite Impulse Response (FIR) filter which performs the final shaping of the signal spectrum and suppresses the aliasing components in the transition band of the HDF. This enables the Decimation filter to implement filters with narrow pass bands and sharp transition bands. The Corrector FIR filter structure used for architecture I is shown in fig.7.The FIR is implemented in a transversal structure using a single Multiplier/Accumulator (MAC) and RAM for storage of data and filter coefficients. The corrector FIR is designed with the decimation factor of two. The 16-bit output of the HDF output register is written into the data RAM on the rising edge of CK_DEC. The Coefficient RAM stores the coefficients for the current FIR filter being implemented. The coefficients are loaded into the Coefficient RAM over the control bus.

B. Architecture II

Cascaded Multistage Decimation Chain

The decimation filter is a block that reduces the data rate from IF to base band domain. Different communication standards require large factor of decimation resulting in large orders of filter networks. Multistage decimation reduces the overall complexity of system, by decomposing the decimation factor in to several sub factors. Thus, each stage requires lower order filters. However, the use of several stages will increase hardware complexity. FIR filter are used in down converters because some modulation schemes requires linear phase[10]. In wireless communication transceivers, the battery life must be maximized. Therefore, high performance blocks with low power consumption and small area are required. The implementation of decimation filter for each standard on a single device is very demanding in terms of overall area and power dissipation. However, with an efficient decomposition of decimation factor and considering common blocks between different communication standards, it is possible to have an efficient design of multi-standard transceivers. Thus, few different blocks could be implemented in a configurable fashion to meet the multi-standard filter circuits requirement.

1) Decimation Chain Structure:

Fig.8 shows the Cascaded Multistage Decimation Chain architecture for two different standards with the decimation factors of 8 and 32. The aim of this architecture is to reduce multiplication operations. To reach this goal, multiplier-less comb filters are used for the first stage similar to architecture I[7]. On simulations, the last two stages of each standard cannot be comb filters, because they don't remove the inband noise level sufficiently. That's why, it was decided to use half band filters for the two last stages. They exhibited good results and excellent out-of-band signal attenuation. The proposed architecture II supports three comb filter stages and 4 stages of half band filters to meet multi-standard requirements. Since the first comb filter stage is used commonly for both the standards, this architecture considerably reduces the area and power of the multi-standard transceiver.

2) CIC Filter Structure:

The fifth order CIC filter structure resembles as that of figure 4 shown in architecture I but the implementation of CIC filter integrators and differentiators stages of architecture II differs from architecture I. Fig.9 shows the basic integrator stage of CIC filter used in this architecture in its Z transform and its equivalent digital circuit in HDL. Thus the single accumulator (Integrator) unit is implemented in HDL using 14-bit adder and a register by avoiding complex multiplexer stages ,when compared with architecture I. In a similar fashion, the differentiator (Comb filter) stage of CIC filter in Z domain and its digital equivalent circuit are represented as shown in fig.10. Thus the comb stage is designed in HDL using a subtractor and a register networks. This architecture results in a considerable reduction in area and power ,when compared to the first architecture. Simulation environment states that further reduction in area and power can be achieved by changing the encoding scheme of filter coefficients from conventional binary number system to Canonic Signed Digit (CSD) Number system.

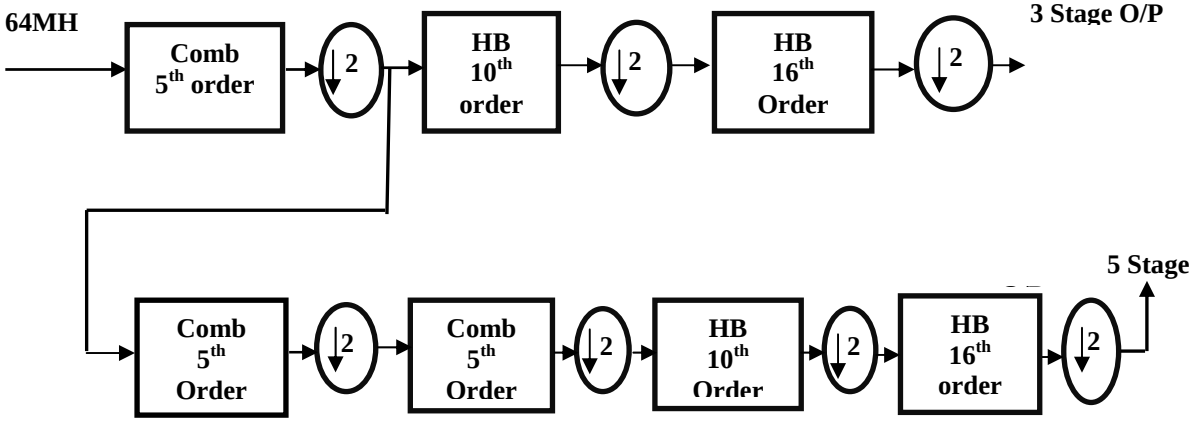

Fig. 8. Cascaded Multistage Decimation Chain Architecture

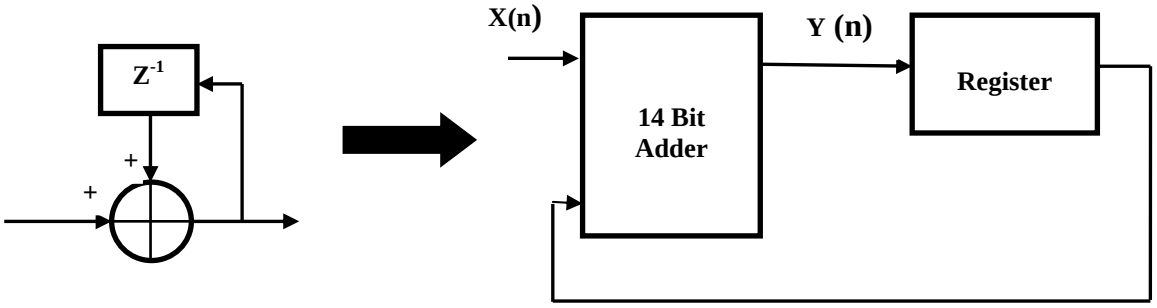

Fig.9.Accumulator in Z-transform and its Digital Circuit Implementation

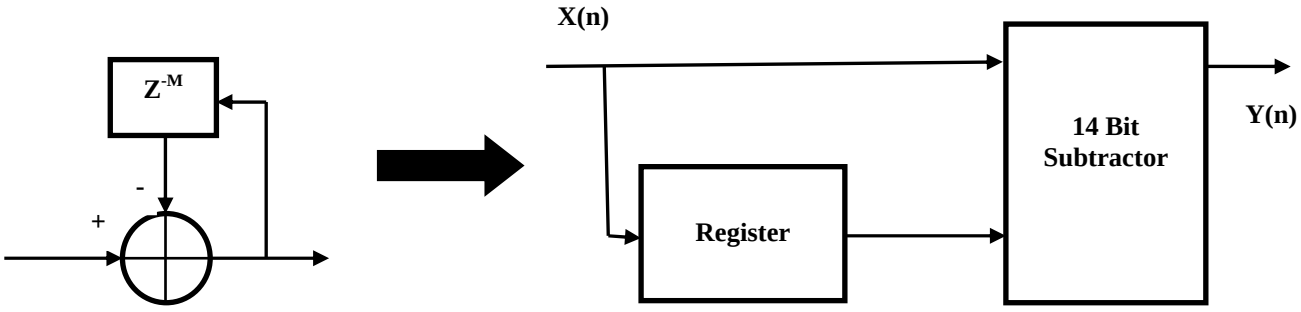

Fig.10. Differentiator in Z-transform and its Digital Circuit Implementation

3) Half Band FIR Filter:

The CIC filter is followed by an half band FIR filter for further down-sampling .The half band FIR filter is used instead of another CIC due to the fact that the pass band of CIC consists of distortions and the half band FIR can be designed in such a way that its frequency response compensates for the distortions created by CIC stages. Since the down-sampling rate of half band filter is chosen to be 2, special type of symmetric coefficients type FIR filter can be used for the architecture II meaning that the coefficients of an odd N tap (N-1 order) half band FIR can be represented by *Ceil [(N-1)/4] +1* numbers[9]. The half band filter significantly reduces the hardware resources needed. The half band filter structure is shown in fig.11.The order of the half band filter used in this design is 14(15 taps) with the filter coefficients quantized for 8-bit precision.

V. CO-EFFICIENT REALIZATION USING CSD REPRESENTATIONS

The CSD representation is a radix-2 signed digit system with the digit set (1,0, _1). For any binary number, the CSD representation is unique and it satisfies the following two properties: first property is that the number of non zero digits are minimal and the second property is that adjacent two digits can never be nonzero digits i.e. the product of adjacent two digits will always be zero. This representation is widely used in multiplier

less implementations of filter design with respect to filter coefficients because it reduces the hardware requirements due to the minimum number of non-zero digits. Any N digit number in CSD format has at most (N+1)/2 non-zero digits thus requiring only that much number of adders/ subtractors. On an average, the number of non-zero digits in CSD is reduced by 33%, when compared with the conventional binary number system. To obtain the CSD representation of a number, start processing its binary representation from the least significant digit to the most significant digit and replace repeatedly all the sequences found as 01…1 by a sequence 10…01 with same number of digits[6]. The conversion table shown in Table I is used to obtain the CSD number of a given binary number.

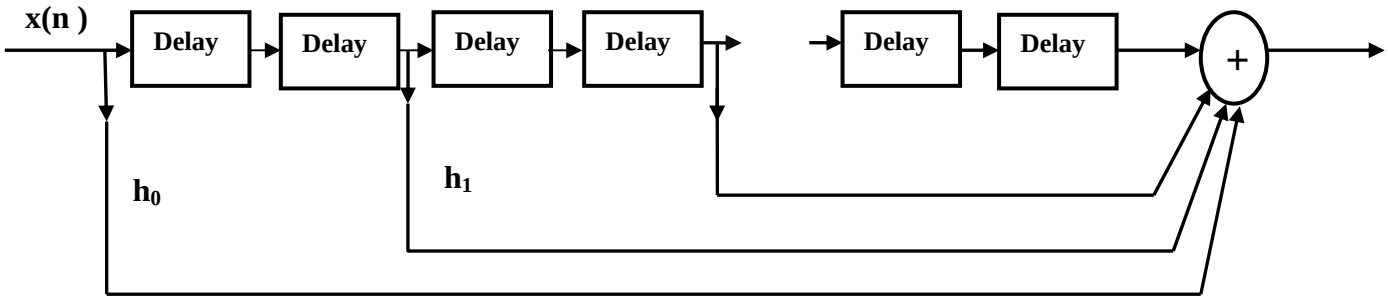

Fig.11. Structure of Half Band Filter

TABLE I
CSD Conversion Table

Inputs			Outputs	
State	b_{i+1}	b_i	c_i	**Next State**
0	0	0	0	0
0	0	1	1	0
0	1	0	0	0
0	1	1	-1	1
1	0	0	1	0
1	0	1	0	1
1	1	0	-1	1
1	0	1	0	1

If the second property of CSD is relaxed, then it leads to an encoding scheme called Minimum Signed Digit (MSD) representation. Although CSD representation is optimal for one constant (filter coefficient-in our case) and it provides unique solution, it is not suitable for common sub-expression procedures of multiple constants. As the CSD representation is unique, it has received much attention and there are many methods of converting a given binary number into the CSD representation. In general, the MSD representation providing multiple representations yielding the same value is more flexible than the CSD representation. This redundancy can result in smaller hardware units than those generated from the CSD representation ,provided appropriate MSD representation is selected for each constant.

VI. SIMULATION RESULTS

The decimation filter design specification is shown in Table II.The input signal frequency is chosen as 64 MHz and the decimation factors are chosen to be 8 and 32 respectively for the multi-standard structures. The pass band of the filter circuit with the decimation factors of 8 and 32 will be 8 MHz and 2 MHz respectively. The pass band ripple and the stop attenuation are taken to be 0.001 and -60 dB. The filter circuit performance has been tested first using Matlab and the filter co-efficients are derived as per the given specifications of Table 6.1. For the implementation of decimation filter architectures in Spartan FPGA, the filter coefficients derived from Matlab are encoded in conventional binary number system and CSD representations. In both the architectures, the overall multistage filter networks are implemented on Xilinx Spartan FPGA .The area in terms of total gate count is analyzed for the architectures and the power analysis are carried out using the power estimating tool Xilinx Xpower Analyzer.Fig.12-15 describes the MATLAB outputs of a conventional decimation filter network. The coefficients derived from MATLAB are converted to CSD form and the performance of the decimation filter architectures are tested using modelsim and the implementation done using SPARTAN FPGA. Table III shows the comparison results of both decimation filter architectures in terms of total gate count, Number of slices, LUTs, IOBs, flip-flops and power consumption with respect to conventional and CSD number system.

TABLE II
Decimation Filter Specification

Specification Parameters	Architecture I	Architecture II
Decimation Factor	8	32
Pass Band	0 to 8MHz	0 to 2MHz
Pass Band Ripple	0.001	0.001
Cut Off Frequency	8.4 MHz	2.4 MHz
Stop Band Attenuation	-60 dB	-60 dB
Output Word Length	16 bits	16 bits

TABLE III
Comparison of Decimation Filter Architectures

S.No.	Architecture Type	Number System Representation	Total Gate Count	No. of Slices	No. of FF	No. of LUT	Logic	IOB	Total Power (mW)
1.	**(I)** Two Stage Decimation Filter	Conventional Number System	17624	554	492	882	770	207	1278
2.	**(II)** Cascaded Multistage Decimation Chain		4279	467	392	442	278	36	57.45
3.	**(II)** Cascaded Multistage Decimation Chain	Canonic Signed Digit (CSD)	3986	235	279	337	278	36	50.11

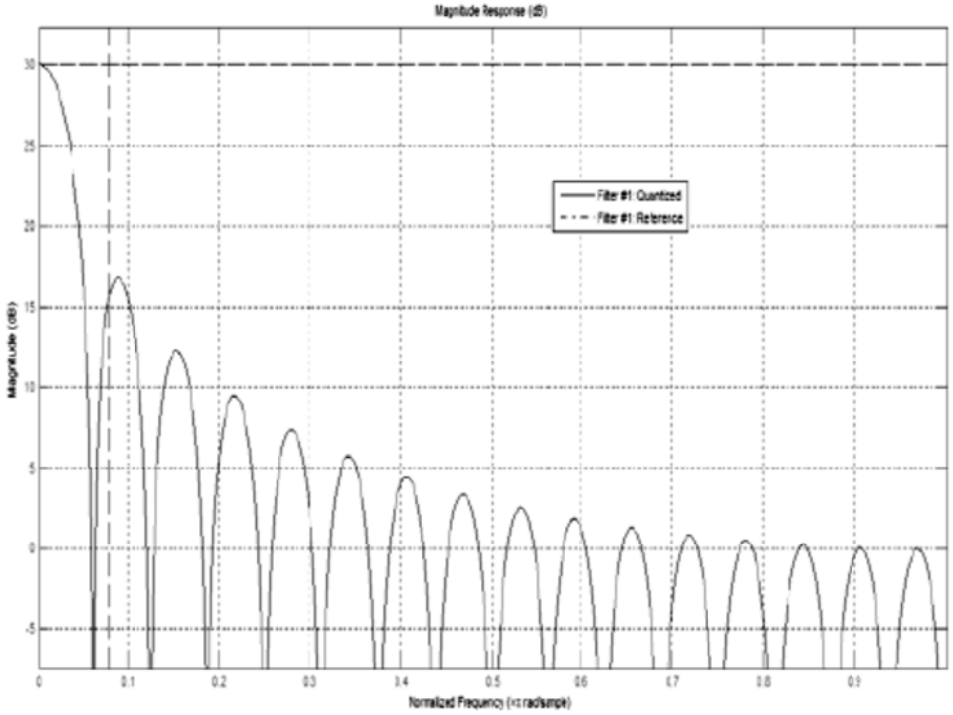

Fig.12. Frequency Response of CIC Filter

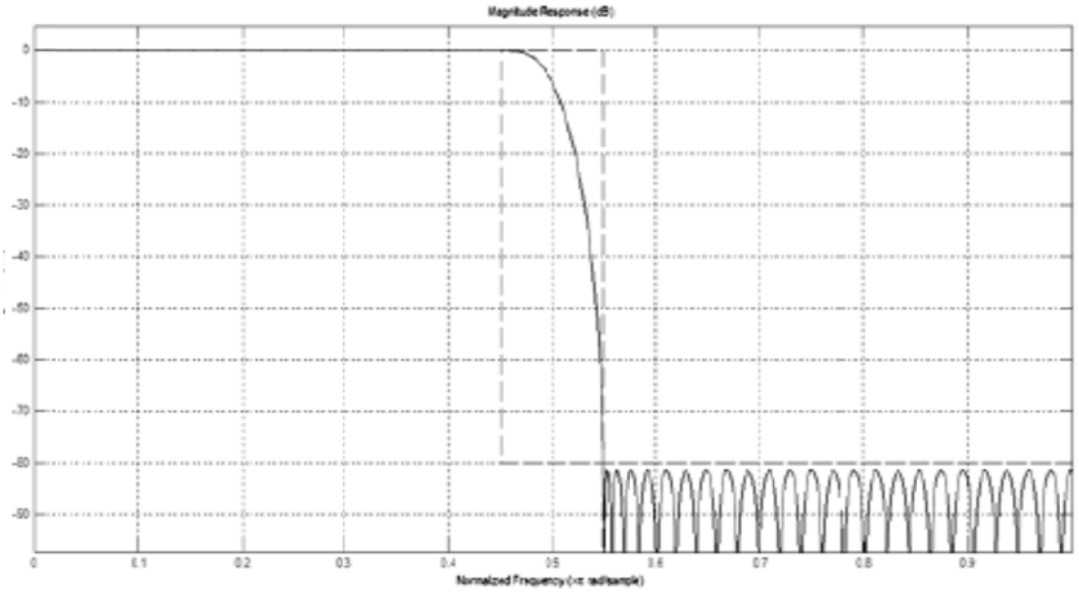

Fig.13. Frequency Response of Half Band Filter

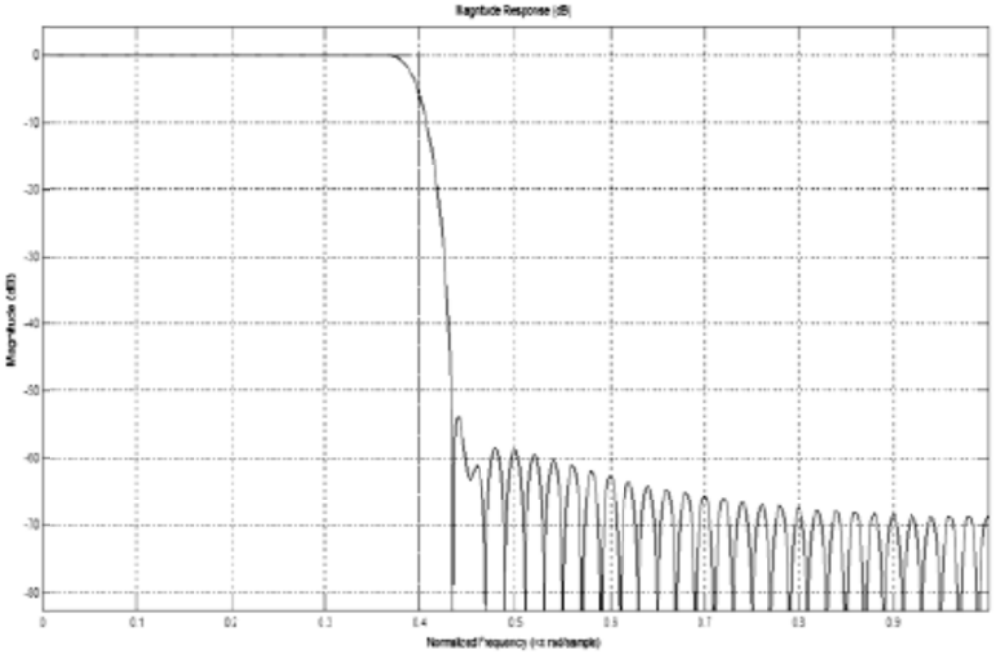

Fig.14. Frequency Response of Decimation Filter

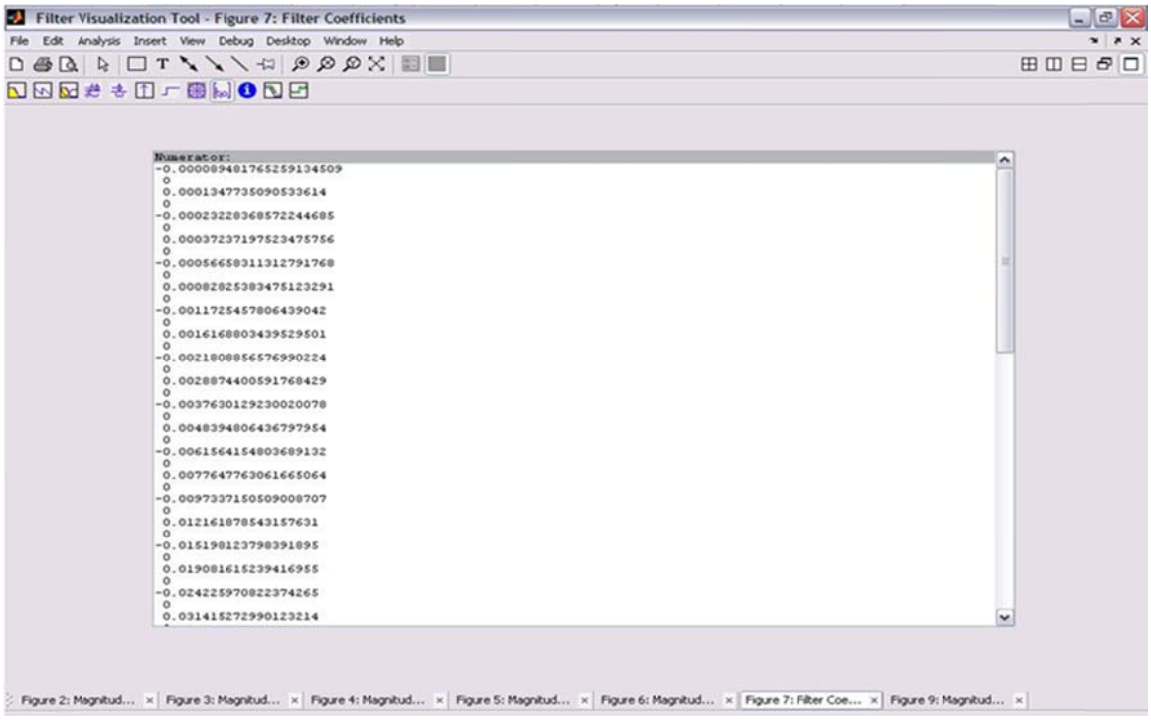

Fig.15. Filter Coefficients of Half Band Filter

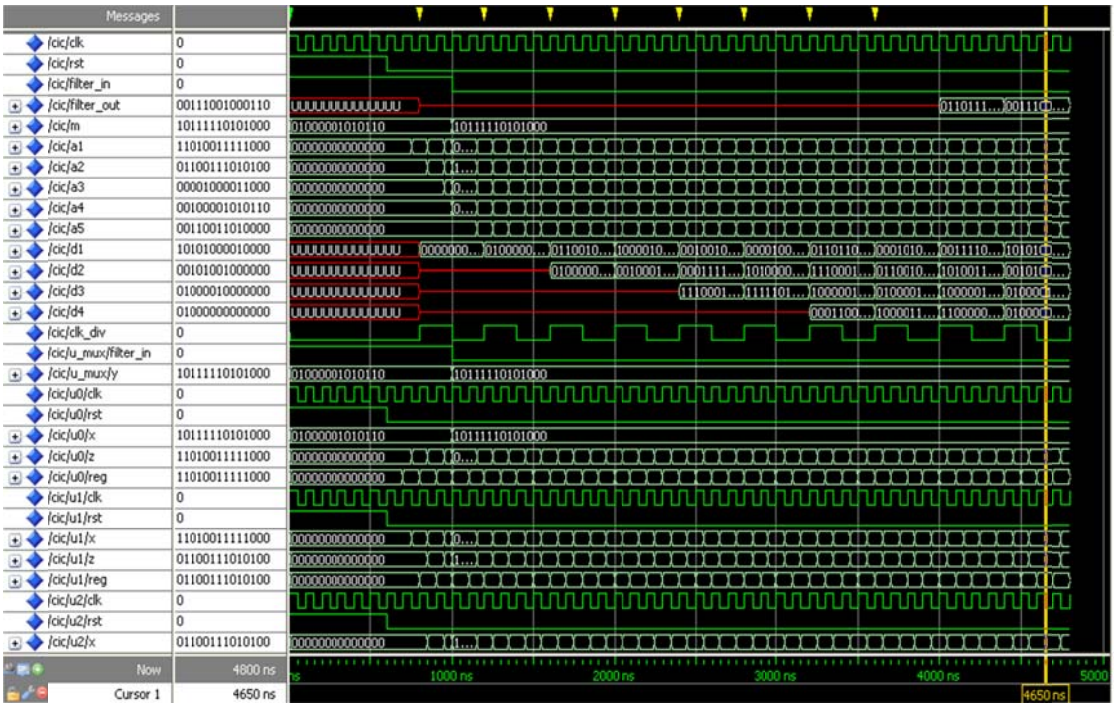

Fig.16. Simulation Result of Five Stage Comb Filter Output

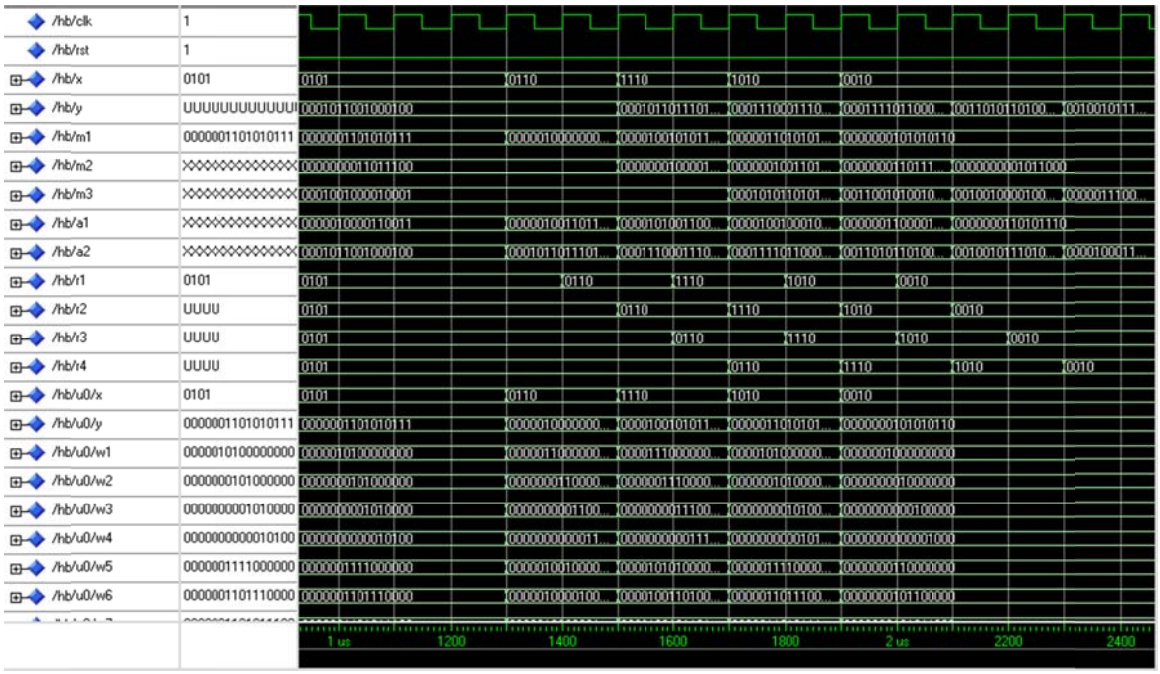

Fig.17. Simulation Result of Half-band Filter using CSD Representation

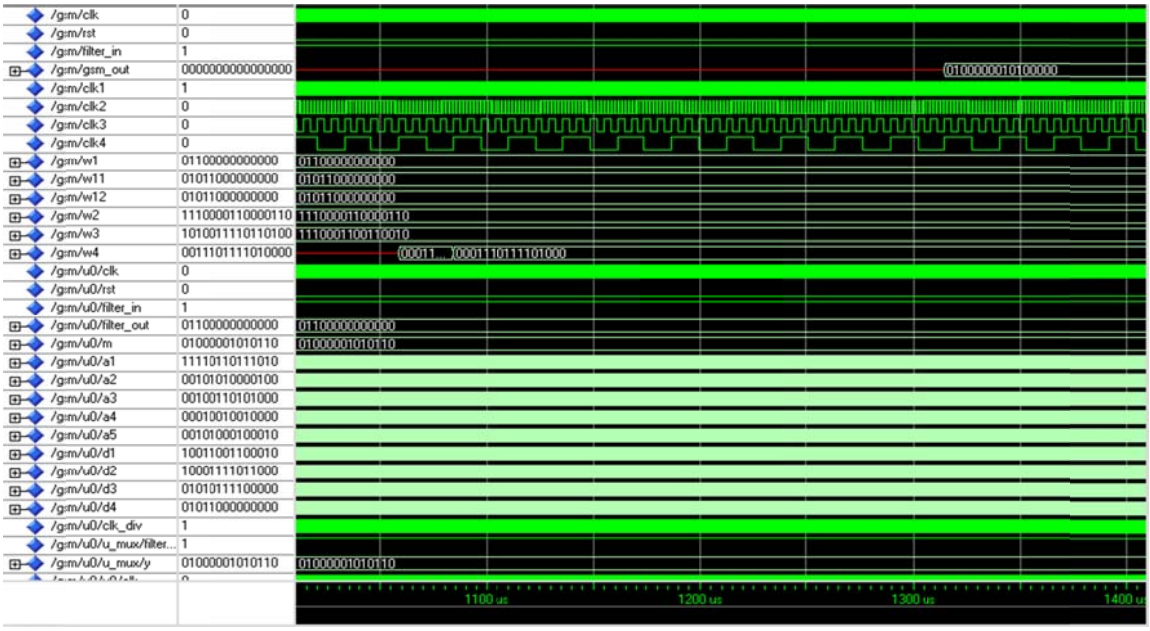

Fig.18. Simulation Result of Decimation Filter for Architecture I

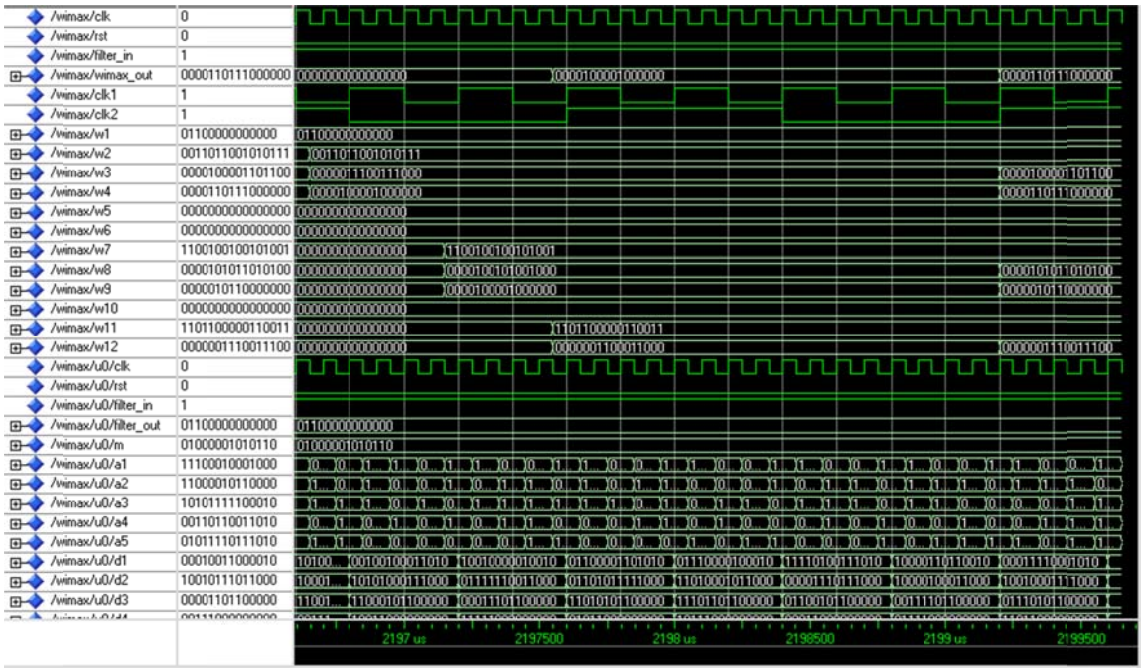

Fig.19. Simulation Result of Decimation Filter for Architecture II

VII. CONCLUSION

Both the decimation filter architectures use the same CIC filter (Comb) network. Simulation results reveals that the total gate count of the decimation filter with MAC unit (two stage decimator) and Cascaded Multistage Decimation Chain architectures are 17624 and 4279. Further reduction in gate count can be achieved by using CSD representations for half band filter coefficients and it is identified to be 3986. The power dissipation of the two stage decimator and the Multistage Cascaded Chain architectures are found to be 1278 mW and 57.45mW respectively. Using CSD representation for half band filters show considerable reduction in power dissipation of Cascaded Multistage Decimation Chain architecture and it is found to be 50.11mW. Future work focuses on implementation of architectures using Minimum Signed Digit (MSD) representation of filter coefficients. The MSD number system is appropriate in finding common sub expressions of multiple constants. The advantage of using the MSD representation for a coefficient results from increasing the possibilities of sharing partial terms between coefficients. Since the MSD number system has a significant reduction effect on the number of additions in the decomposed multiplication block and eliminates the number of common sub-expressions.

REFERENCES

[1] Shahana T . K, Babita ,R Jose Jacob and Sreela Sasi "Decimation Filter Design Toolbox for Multi-Standard Wireless Transceivers using MATLAB" PP 154 -163, International Journal of Signal Processing 5,2009.

[2] Massimiliano Laddomada "Design of Multistage Decimation Filters using Cyclotomic Polynomials: Optimization and Design Issues", IEEE Transactions on Circuits & Systems,VOL.55, NO. 7, AUGUST 2008.

[3] Guo-Ming Sung, Hsiang-Yuan Hsieh "An ASIC Design for Decimation Filter with CSD Representation"International Symposium on Intelligent Signal Processing & Communication Systems Swissôtel Le Concorde, Bangkok,Thailand,2008.

[4] R. A. Losada and R. Lyons, "Reducing CIC filter complexity,"IEEE Signal Process. Mag. Vol. 23, no.4,pp.124– 126, Jul., 2006.

[5] Ling Zhang, Vinay Nadig and Mohammed Ismail, "A High Order Multi-bit ΣΔ Modulator for Multi-Standard Wireless Receiver",IEEE Midwest International Symposium on Circuits and Systems, pp. III-379-382, 2004.

[6] S.-M. Kim, J.-G. Chung, Parhi, K.K.,"Low Error Fixed-Width CSD Multiplier with Efficient Sign Extension" IEEE Transactions on Circuits & Systems II: Analog & Digital Signal Processing, Vol. 50, no. 12, Dec. 2003.

[7] Y. Gao, J. Tenhunen, and H. Tenhunen, "A Fifth-Order Comb Decimation Filter for Multi-standard Transceiver Applications," in Proc. Geneva, Switzerland, May 28–31, 2000, pp. III-89–III-92.

[8] S. Chu and C. S. Burrus,"Multi-rate Filter Designs using Comb Filters,"IEEE Transactions on Circuits Syst., vol. CAS-31, no. 11, pp. 913–924, Nov. 1984.

[9] R. E. Crochiere and L. R. Rabiner, Multirate Digital Signal Processing, Upper Saddle River, NJ: Prentice-Hall,1983.

[10] E. B. Hogenauer, "An Economical Class of Digital Filters for Decimation and Interpolation," IEEE Trans. Acoust., Speech, signal Process., vol. ASSP-29, no. 2, pp. 155–162, Apr. 1981.

AUTHORS PROFILE

R. Latha (Rajagopalan Latha) obtained his Bachelor's degree in Electronics and Communication Engineering and Master's degree in Applied Electronics from Bharathiar University , TamilNadu, India and currently pursuing her PhD degree under Anna University,Chennai, TamilNadu, India. Currently, she is working as an Academician at Christ University- Faculty of Engineering , Bangalore , in the department of Electronics and Communication Engineering. Her specializations include Microelectronics, Microcontroller Architectures, Digital Signal Processing and VLSI design . Her current research interests are in the area of Multi-rate Digital filter design, wireless Communication and architecture optimization using HDL's.

Dr. P.T. Vanathi received the BE degree in Electronics and Communication Engineering and ME degree from PSG College of Technology, Coimbatore in the year 1985 and 1991 respectively. She completed her PhD in the area of Speech Signal Processing in the year 2002 from Bharathiar University, Coimbatore.

She has around 24 years of teaching and research experience. Her research interests include Soft computing, Speech Signal Processing, Wireless Sensor Networks and VLSI Design. Under her guidance 6 Research Scholars have completed their Ph.D. She is currently guiding 8 Research Scholars in various fields of Electronics and Communication Engineering. She is currently working as an Associate Professor in the ECE department of PSG College of Technology. She was the Co coordinator for SSS-Impact Project funded by Swiss Development Cooperation and Government of India. She was the Co-Coordinator for the VLSI - SMDP II project funded by Ministry of Communication and Information Technology, New Delhi during 2005-2009. She was instrumental in the fabrication of Integrated Circuit jointly with Indian Institute of Science, NIT, Surathakal and BESU, Howrah under the India Chip Programme in the year 2008. She was also a Coordinator for the INTEL Academic programme during 2007-2009 and a member of Core Faculty Group (CFG) of INTEL Multicore project during 2009. She has coordinated the First National Conference on VLSI Design and Testing in the year 2003 and organized the Second National conference on VLSI Design in the year 2006. She is a life member of ISTE. She has jointly coordinated a Research project funded by AICTE with Dr. K. Gunavathi. She has organized short term courses in the area of VLSI Design and Microcontroller and its applications. She has published 60 papers in national and international journals and 93 papers in national and international conference publications.