# A Perspective Review of Tunnel Field Effect Transistor with Steeper Switching Behavior and Low off Current ($I_{OFF}$) for Ultra Low Power Applications

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**Abstract - With down Scaling of MOSFET to nanometer dimensions, the OFF-state leakage current($I_{off}$) increases exponentially due to the non scalability of threshold voltage since the Subthreshold Swing(S) is limited to 60mV/decade. Steep Subthreshold Swing transistors based on Band to Band Tunneling (BTBT) are analyzed to improve the performance of the circuit for low power applications. This review paper discuss about various structures and modeling of Tunnel Field Effect Transistor(TFET) which replaces CMOS for greater energy efficiency which is considered to be the most critical design parameter for ubiquitous and mobile computing systems.**

**Keywords –** Down Scaling, Band to Band Tunneling (BTBT), Subthreshold Swing(S), Tunnel Field Effect Transistor(TFET)

## I. INTRODUCTION

As MOSFETs are aggressively scaled, their performance is severely limited by short channel effects such as Drain Induced Barrier Lowering (DIBL), punch through, enhanced leakage current and reduce device performance [1]. The conventional metal oxide semiconductor field effect transistor (MOSFET) may not be suitable for future low standby power (LSTP) applications due to its high off-state current as the sub-threshold swing is theoretically limited to 60 mV/decade. Tunnel field effect transistor (TFET) based on gate controlled band to band tunneling has attracted attention for such applications due to its extremely small Subthreshold swing (much less than 60mV/decade).The leakage power is strongly influenced by the subthreshold swing of a device defined by the drain-to-source current under an applied gate-to-source voltage $V_{GS}$. The *S* indicates the minimum amount of gate-voltage reduction necessary to lower the Subthreshold current by a factor of ten.[2] In order to meet the ON-current $I_{ON}$ requirements, the threshold voltage $V_{TH}$ needs to be scaled with $V_{DD}$. However, $I_{OFF}$ exponentially increases with $V_{TH}$ reduction and is given by

$$I_{OFF} = I_{DS}.10^{-V_{TH}/S} \quad (1)$$

With $S = \eta(kT/q)\ln 10$ and $\eta = 1 + (C_{dep}/C_{ox})$. In (1), S is the Subthreshold slope of the device and depends on junction capacitance *C*dep and gate capacitance *C*ox. S is a nonscalable parameter, and minimum Subthreshold swing $S_{min}$ is 60mV/dec at room temperature. Hence, $V_{TH}$ has become a nonscalable parameter to limit the $I_{OFF}$.[3] However, due to the short-channel effects (SCEs), S is far worse than an ideal value of 60 mV/dec. In order to limit $I_{OFF}$ while scaling down $V_{TH}$, it is important to look for new device structures that achieve subthreshold swing below 60 mV/dec. Fig. 1 shows the minimum reported values of S for various classical and nonclassical CMOS, as well as nonsilicon solid-state devices [4]–[8].

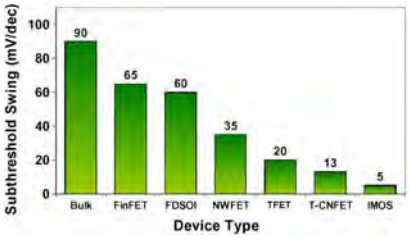



Fig. 1. Subthreshold swings (*S*) reported for various CMOS and emerging solid-state devices. From [2]

It can be observed that all of the CMOS-based transistors [Bulk, FinFET, and fully-depleted silicon-on-insulator (FDSOI)] have *S* values ≥ 60 mV/dec (= 2.3 kT/q) at room temperature, while the nanowire field-effect transistor (NWFET) [9], the carbon nanotube based tunnel field-effect transistor (T-CNFET) [7],[8], and the

Impact-Ionization MOS-based transistor (IMOS) [6] have lower values of *S* (sub-kT/q). Among the new generation of sub-kT/q transistor, TFET is performance better due to low IOFF and chip implementation is similar to CMOS.

Previous works on TFET experimentally shown that ON-currents are unacceptably low for a technology that would like to replace the conventional MOSFET. While OFF-currents are in the range of femtoamperes [9] or picoamperes [10], [11] and ON-currents limited to the nanoamperes range [10], [11]. Looking at the 2005 ITRS [13], the Tunnel FET technology fits best into the Low Standby Power (LSTP) category. For the 50-nm node, an ON-current of 0.612 mA is required with an OFF-current of 10 pA. New Tunnel FET designs will be needed, in order to attain this Ion without sacrificing $I_{OFF}$.

## II. DEVICE OPERATION AND STRUCTURE

Tunnel FETs are gated p-i-n diodes. To switch the device on, the diode is reverse biased, and a voltage is applied to the gate. In order to be consistent with MOSFET technology, the names of the device terminals are chosen such that voltages are applied in a similar way for Tunnel FET operation. Since a reverse bias is needed across the p-i-n structure in order to create tunneling, and since an NMOS operates when positive voltages are applied to the drain and gate, the n-region of a Tunnel FET is referred to as its drain, and the p+ region as its source for an n-type device. Fig.2 shows the basic device structure for a typical p-i-n Tunnel FET. The structure shown is an n-type device, with a p+ source and an n+ drain. In a p-type Tunnel FET, the source would be doped n+ and the drain would be doped p+. Tunnel FETs have a metal gate with a work function of 4.5eV

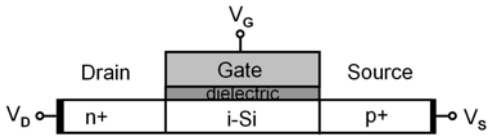



Fig. 2. A simple Tunnel FET device structure, an n-i-p diode with one gate. From [14]

The working principle of conventional TFET and band diagrams are shown in Fig. 2. In the absence of a gate voltage (non-conducting region), the tunneling barrier width is large enough to give extremely small current ($I_{OFF}$). However, on application of positive gate voltage, the bands in the intrinsic (lowly doped) region are pulled downwards and a tunneling barrier is created between source and channel. Due to the reduction in tunneling width and electric fields produced, Zener tunneling of electrons takes place from the valance band of the source to the conduction band of the channel and the device turns ON.

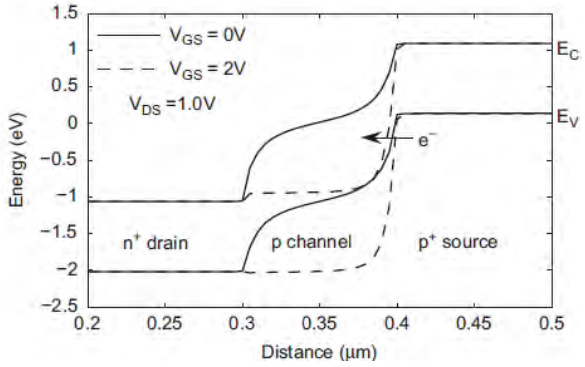



Fig.3 Simulated band diagrams of the n-type conventional TFET in non-conducting and conducting regions. From [15]

One should note that this behavior is an analogous to NMOS in the CMOS technology. For a Tunnel FET, the ON current is proportional to the electron/hole transmission probability T(E) in the BTBT mechanism, which is given by [16]:

$$T(E) = \exp\left( \frac{4\sqrt{2m^*}\,Eg^{3/2}}{3|e|\hbar(Eg+\Delta\Phi)} \sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{ox}} t_{ox} t_{Si}} \right) \Delta\Phi \qquad (2)$$

Where m* is the carrier effective mass, e is the electron charge, Eg is the bandgap, $\Delta\Phi$ is the energy range over which tunneling can take place, and $t_{ox}$, $t_{Si}$, $\varepsilon_{ox}$ and $\varepsilon_{Si}$ are the oxide and silicon film thickness and dielectric constants, respectively. This equation shows decreasing oxide thickness ($t_{ox}$) [16], increasing oxide dielectric constant ($\varepsilon_{ox}$), and reducing band gap ($E_g$), will enhance the performance of the device. Boucart and Ionescu[14] have proposed the use of high-k materials as the gate dielectric (high $\varepsilon_{ox}$ in Eq.(1)) in order to increase ON current($I_{ON}$).

## III. TUNNEL FET CHARACTERISTICS

### *A. Steeper Switching Behavior*

The Subthreshold swing of a device is defined as the change in voltage which must be applied in order to create a one decade increase in the output current, or

$$S = \frac{dVg}{d(\log I_d)}[mV/dec] \tag{3}$$

In a metal–oxide–semiconductor FET (MOSFET), the current-switching process involves the thermionic (temperature-dependent) injection of electrons over an energy barrier. This sets a fundamental limit to the steepness of the transition slope from the off to the on state. The gate voltage required to change the drain current by one order of magnitude when the transistor is operated in the subthreshold region is reflected in the expression of the subthreshold swing, *S*:

$$S = \underbrace{\frac{dV_G}{d\Psi_s}}_{m}\underbrace{\frac{d\Psi_s}{d(\log_{10} I_D)}}_{n} \cong \left(1+\frac{C_d}{C_{ox}}\right)\ln 10\frac{kT}{q} \tag{4}$$

$$\rightarrow \frac{kT}{q}\ln 10 \cong 60mVdecade^{-1} \mid \mathrm{T} = 300\mathrm{K}$$

where $V_G$ is the gate voltage, $I_D$ is the drain current, kT/q is the thermal voltage, and $C_d$ and $C_{ox}$ are the depletion and the oxide capacitances, respectively. The term *m* is the transistor body factor, and *n* is a factor that characterizes the change of the drain current with the surface potential, $\Psi_S$, reflecting the conduction mechanism in the channel. A subthermal *S* would be less than *kT*/*q* ln10 and could be obtained by using new physical principles rather than thermionic injection. As the transistor gate length is reduced, improved performance requires the supply voltage, $V_{DD}$, and simultaneously the threshold voltage, $V_T$, to be lowered to keep the overdrive factor ($V_{DD} - V_T$) high. As a consequence, the leakage current, $I_{OFF}$, increases exponentially because the *S* of a MOSFET is not scalable but has a minimum value of 60 mV per decade (that is, it takes 60 mV to increase the current by one order of magnitude) at room temperature[18].

Another way of reducing the voltage supply without performance loss is to increase the turn-on steepness, which means decreasing the average subthreshold swing, *S*avg defined as:

$$S_{avg} = \frac{V_T - V_{GOFF}}{\log\frac{I_T}{I_{OFF}}} \approx \frac{V_{DD}}{\log\frac{I_{ON}}{I_{OFF}}} \tag{5}$$

Therefore, devices with a steep *S*, called steep-slope switches, are expected to enable $V_{DD}$ scaling. The dependence of swing on gate voltage up to the threshold voltage (taken at $I_{DS} = 10^{-7}$ A/μm) is shown in Fig. 4. The points were generated by taking the swing value ($dV_{GS}/d(\log I_{DS})$) at each point on the $I_{DS}$-$V_{GS}$ curves, fig.4. demonstrates two important things. First, the subthreshold swing of Tunnel FETs is not constant, but rather is a function of gate voltage. And second, at low gate voltages, it is possible for Tunnel FETs to have a subthreshold swing less than the 60 mV/decade MOSFET limit at room temperature and shows that as gate dielectric thickness is reduced, S decreases linearly, and consequentially, ON-current increases exponentially. Swing is smallest at the lowest $V_{GS}$, and increases as $V_{GS}$ increases.

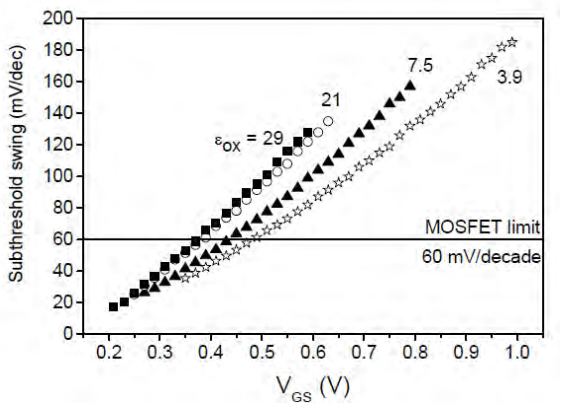



Fig.4. Dependence of the Tunnel FET subthreshold slope on gate voltage for different dielectric constants. From [14]

Comparison of the $I_{DS}V_{GS}$ curves for a typical conventional MOSFET, and for a typical Tunnel FET is shown in fig.5.

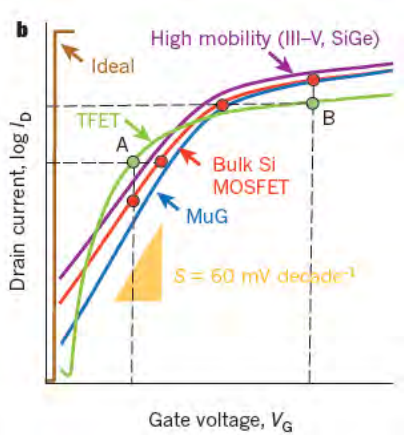



Fig.5. Qualitative comparison of three engineering solutions to improve the characteristics of the bulk silicon MOSFET switch (red): a multigate device (MuG, blue) for improved electrostatics; a high-mobility channel (purple) using group III–V and SiGe materials; and a TFET (green).

A qualitative comparison of some major candidates to improve the characteristics of bulk silicon MOSFET switches: multigate devices for improved electrostatics; high-mobility channels exploiting group III–V and SiGe materials; and TFETs that use quantum-mechanical tunneling is shown in Fig.5. At moderate performance requirements, such as operation point A, TFETs offer not only improved $I_{ON}/I_{OFF}$, but also superior performance (higher $I_{ON}$ at the same voltage) or power savings at the same performance (lower voltage for the same $I_{ON}$) over MOSFETs. However, when a much higher performance is required, such as at operation point B, a MOSFET is the better solution

*B. Band-to-Band Tunneling Transmission*

The simulation of BTBT recently attracted interest as researchers attempt to realize tunneling transistor (TFET) that provides steep switching characteristics. Since T-FET derives its drain current from the band-to-band tunneling at the source–channel junction, the transfer characteristics is not bound by the 60 mV/decade limit in MOSFETs. In TFET, band-to-band tunneling is the principal device physics to be modeled. In addition to the ON-current, the shape of the drain voltage characteristic also determines the manner in which a device is able to charge/discharge a capacitive load. In a MOSFET, the gate voltage modulates the channel barrier height, while the source/drain voltage only provides a lateral field to remove the carriers. In a TFET both the gate and source/drain voltages modulate the lateral electric field at the tunneling junction. It is impossible to de-couple the source/drain voltage from the tunneling current. The result is an exponential Id vs. $V_d$ curve which saturates at higher voltages only when the channel resistance limits current flow. This is fundamental to all lateral BTBT devices. In the simple local BTBT model, the carrier generation rates are calculated primarily from the local E-field only. In one common expression, based on the Kane's derivation,

$$G^{BTBT} = A.E^{\alpha} \exp(-\frac{B}{E}) \tag{6}$$

where E is the electric field and A, B, and a are fitting parameters. This approach is simple and numerically very robust, but ignores recombination due to tunneling, and is apparently unphysical. Hurkx suggested an amendment to the local BTBT model, which adds to (6) a prefactor

$$D = \frac{np - n_i^2}{(n + n_i)(p + p_i)} \tag{7}$$

Hurkx's model accounts for recombination, but is still a local model. When the tunneling rate is high, the local n–p product can greatly exceed $n_i^2$, but this is not allowed in Hurkx expression. The physically correct D factor should use the electron and hole concentration at the start- and end-point of the tunneling path (classical turning points), but this is not possible with a local BTBT model. One clever workaround of this problem is the pseudo-local algorithm, which use the local gradient of quasi-Fermi levels and the local E-field to extrapolate the electron and hole concentration at the classical turning points, and calculate D factor using the extrapolated concentrations.

An expression for the band-to-band tunneling current in Tunnel FETs can be found by using the WKB approximation and taking the tunnel barrier as a triangularly shaped potential barrier as shown in Fig. 6.

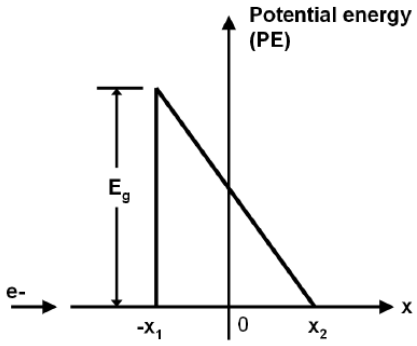



Fig. 6 Band-to-band tunneling can be calculated by approximating the energy barrier width by a triangular potential energy barrier, where the electrons must tunnel through the widest distance at the base of the triangle. Redrawn from [20].

Fig. 7 shows how the band-to-band tunneling behavior of the Tunnel FET acts as a band pass filter that cuts off the low-energy and high-energy tails of the Fermi distribution of the n+-type source. The Fermi-Dirac distribution and Fermi level for the source are first drawn at the left within the source, and the low-energy tail of the distribution is crossed out because no carriers can exist at energies inside the band gap. Then on the channel side, the source Fermi-Dirac distribution is shown again, and this time the high-energy tail is crossed out since those energy levels can't exist inside the band gap of the channel. The result is the version of the distribution shown at the far right, in which only the electrons in the source within the energy range ΔΦ are available for tunneling.

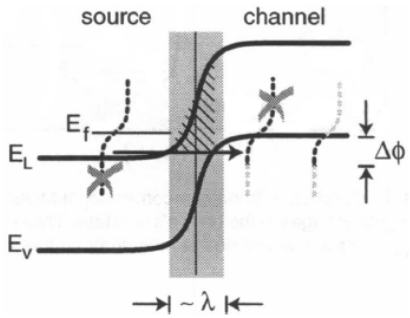



Fig. 7 Energy band cross section of a Tunnel FET showing the triangular barrier approximation within the bands, ΔΦ, the screening length λ, and the filtering behavior of the device in the on-state. From[16]

## IV. NOVEL TFET STRUCTURES TO BOOST ON CURRENT($I_{ON}$)

Tunnel FETs are considered to be an alternative for conventional MOSFETs due to their low leakage currents, less susceptibility to short channel effects (SCEs) and feasibility of integration with standard CMOS process flow. But the maximum ON current for silicon based TFETs demonstrated experimentally is well below the ITRS requirements. .Several works are carried out to improve ION/IOFF ratio, to enhance the ON current various design improvements in terms of bandgap engineering, hetero-junction TFETs, use of strained silicon , novel architectures like carbon nanotube TFETs have been proposed. Fig. 8 shows some of the novel structures to boost $I_{ON.}$

### *A. Single Gate TFET*

The device structure shown in figure 8.a was proposed by kathy Boucart in 2006. It is a lateral n-type Tunnel FET in a thin silicon layer, isolated from the substrate by a dielectric layer. The basic design is a gated p-i- n diode. The tunneling takes place in this device between the intrinsic and p+ regions. To operate these devices, the source is grounded, a low voltage (~0.1V) is applied to the drain, and a voltage is applied to the gate(s). Without a gate voltage, the width of the energy barrier between the intrinsic region and the p+ region is wider than 10nm (the approximate minimum for tunneling current to take place) and the device is in the off-state. As positive gate voltage increases, the bands in the intrinsic region are pushed down in energy, narrowing the tunneling barrier, and allowing tunneling current to flow. Since a reverse bias is needed across the p-i-n structure in order to create tunneling, and since an NMOS operates when positive voltages are applied to the drain and gate, the n-region is referred to as the drain, and the p+ region is the source. To maximize the on-current and to keep off-current low, it is desirable to have high source doping compared to drain doping ($N_{source}$ = $1x10^{20}/cm^3$,$N_{intrinsic}$ = $1x10^{17}/cm^3$,$N_{Drain}$=$5x10^{18}/cm^3$). For Silicon-based TFETS on-currents of about $I_{ON}$=100μA/μm are achieved with $I_{ON}/I_{OFF}$ ratios of about $10^6$ for sub 0.5V supply voltages [18].

*B. Double Gate TFET*

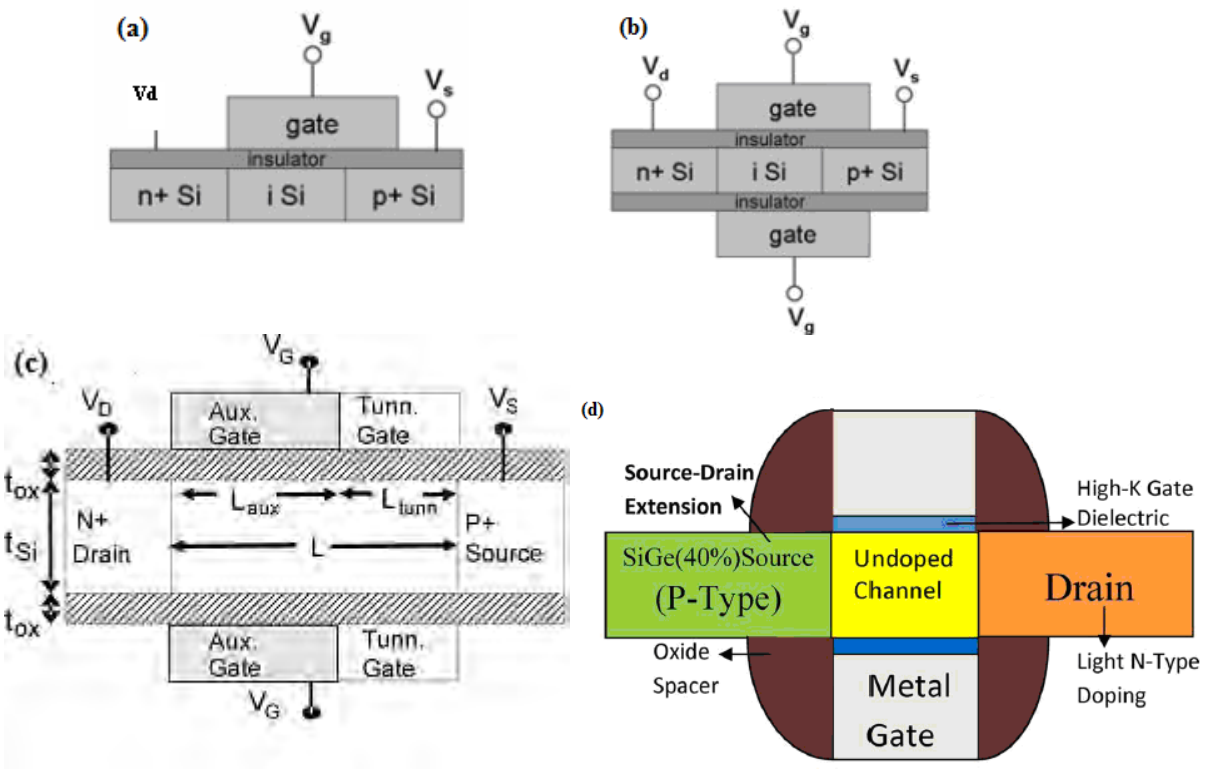
As per the ITRS Roadmap, TFET is best for LSTP(Low Standby Power) category. For the 50 nm node, an on-current of 0.612 mA is required, with an off-current of 10 pA. TFET with double gate and high-K dielectric with optimized silicon body thickness design was proposed by Kathy Boucart in order to attain this Ion without sacrificing $I_{OFF}$ shown in fig.8.b. The Tunnel FET uses a high-K gate dielectric with a dielectric constant of 29 and the on-current will be doubled due to the added gate. The double gate and high-K dielectric raise on-current to 1 mA at Vg = 1.2 V, and provide a corresponding improvement in the average subthreshold swing, as low as 52 mV/dec and a minimum point slope of 18mV/dec and maximizing the ratio $I_{ON}/I_{OFF}$ to $10^{13}$[18].However the ON current of the DG TFET is still to be improved.

*C. Dual Material Gate (DMG) in a Double-Gate TFET (DGTFET)*

Sneh Saurabh [21] proposed a new DMDG TFET, incorporating with DMG structure and DG structure as shown in fig.8.c. This device offers excellent device performance like increased ON current, reduced OFF current, improved subthreshold slop and immunity against DIBL effects. This design is able to deliver a high $I_{ON}$ of about 10 $\mu$A/$\mu$m, $I_{OFF}$ of about 1 fA/$\mu$m and subthreshold Swing of about 58 mV/dec. But the $I_{ON}$ is less when compared to that of the MOSFET. To maximize the $I_{ON}$ Sneh Saurabh [21] demonstrated that DMG technique in an Strained DGTFET(SDGTFET) with a high-*k* gate dielectric not only achieve an improved $I_{ON}$ and SSAVG but also improve the overall performance of the Device. Work function of the auxillary gate ($\Phi$aux) and tunnel-gate work function ($\Phi$tunnel) can be adjusted for better $I_{OFF}$, $I_{ON}$, and $V_T$ tradeoffs. The DMG-SDGTFET is able to deliver a high $I_{ON}$ = 351 µA/µm, $I_{OFF}$ < 1 fA/µm, the ratio of $I_{ON}/I_{OFF}$ is about $3 \times 10^{12}$, and $V_T$ = 0.20 V. The SSAVG improves from 34 mV/dec in an SMG-SDGTFET to 21 mV/dec in a DMG-SDGTFET

*D. SiGe lateral heterostructure TFET(HTFET)*

Tejas Krishnamohan, proposed that the lateral heterostructure TFET Fig.8.d with s-Ge/Si interface at the Source-side can significantly suppress the drain side tunneling during OFF-state due to the large bandgap of Si (compared to Ge), while maintaing high drive currents in ON-state. In the paper[23] it is experimentally demonstrated that a DG, s-Ge, TFET exhibit $I_{ON}$=~300uA/um and SS~50mV/dec. It is also proved that the lateral heterostructure is the most effective and scalable approach to solve the ambipolar issue in TFETs[23].



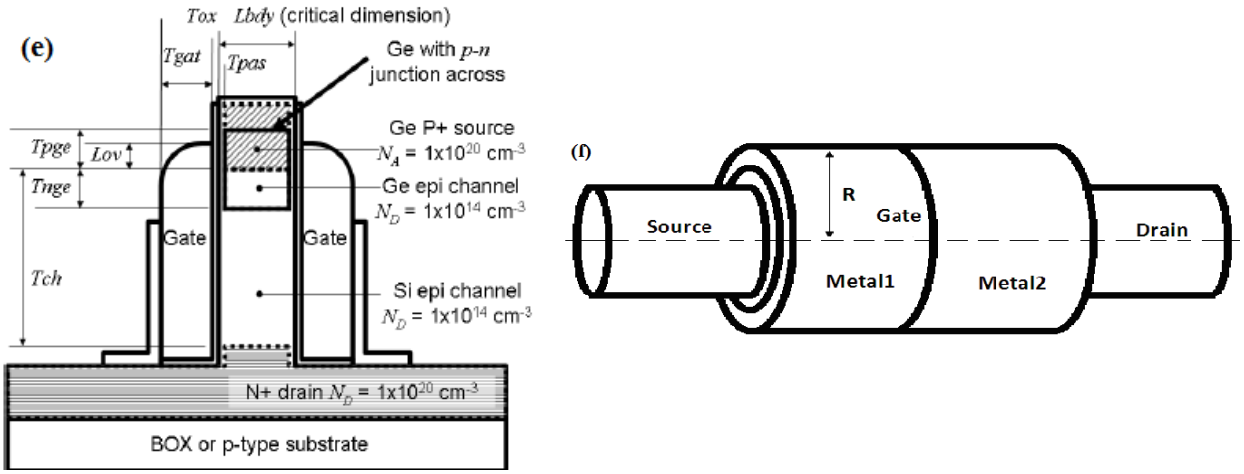



Fig. 8. Device structure of the (a) single-gate TFET[18], (b) double-gate TFET[18], (c) DMG-DGTFET[21], (d) SiGe lateral heterostructure TFET(HTFET)with 40% Germanuim at the source[23], (e) Vertical TFE[22]T, (f) n-Channel Dual Material Surrounding Gate n-TFET[24]

### *E. Vertical TFET*

In Conventional TFET it is very difficult to maintain good subthreshold characteristics and high $I_{ON}/I_{OFF}$ in deep sub-micron dimension due to the electrostatic effect from the drain. Min-Chul Sun[22] proposed the structure vertical-channel TFET fig.8.e[22] the vertical structure allows a long enough channel to minimize the electrostatic effect of the drain region without any expense of scalability. Advantage of vertical structure is that the channel can be isolated from the substrate without silicon-on-insulator (SOI) substrate. Also, the embedded Ge region that source/channel *p-n* junction is formed across maximizes the tunneling current by making best use of the depletion region for tunneling. However, the fabrication of this structure will face several practical challenges. One of them is the well-known instability of Ge/SiO2 interface .Since the interface is so unstable to form significant interfacial state even by $500^0$C.Heavy doping of donor above $1\times10^{18}$ cm$^{-3}$ on the *n*-type region of Ge also improves the switching property and drain current. While the vertical configuration got rid of channel-length limitation and extended the scalability below 10 nm in minimum feature size, the optimized embedded Ge-junction drastically improved $I_{ON}/I_{OFF}$, S and on-current. By this method $I_{ON}/I_{OFF}$ greater than $10^6$, 50 mV/decade of S and $I_{ON}$ of 151.5 μA/um when $V_{DS}$ = 0.9 V and $V_G$ - $V_T$ = 0.7 V with a 10-nm minimum feature design is obtained. Even more improvement in the drive current and switching characteristics is expected once we can use such materials of effectively smaller bandgap to form the source junction.

### *F. n-Channel Dual Material Surrounding Gate n-TFET*

TFET suffers from low ON-current because of its small amount of band to band tunneling efficiency in the large band gap silicon body. Various structural reformation techniques has been proposed to improve the $I_{ON}$, Sayani Ghosh[24] has proposed the 2D model of surface potential for dual material surrounding gate tunneling field effect transistor. The fig.8.f shows the structure of gate all around(GAA) TFET with silicon body radius R=10nm, Metal 1 region L1=20 nm which is implanted from the initial point of the channel, Metal 2 region channel Length L=50 nm and oxide($SiO_2$) thickness $t_{ox}$=2nm.Sayani Ghosh has shown that device $I_{ON}$ increases with the use of relatively low work function gate at source side which significantly narrowed tunneling width .

Table I
Comparison of $I_{ON}$ for various design structure

| Reference | Device Structure | Ion ($\mu$A/$\mu$m) |
|---|---|---|
| [25] | GOI pTFET | 1 |
| [26] | Si pTFET | 0.15 |
| [27] | SOI pTFET with NiSi dopant segregation | 0.47 |
| [28] | Strained Si NW pTFET with NiSi dopant segregation | 7 |
| [21] | DMG-DGTFET | 10 |
| [22] | Vertical TFET | 151.5 |
| [21] | DMG-Strained DGTFET | 351 |

## V. TFET FOR ULTRA LOW POWER APPLICATIONS

With down scaling of MOSFET, the static power has become a dominant component in total power consumption since $V_{TH}$ reduction is critical to lower supply voltage, $I_{OFF}$ increases exponentially as the threshold voltage is reduced. Sub-threshold slope of CMOS is limited to 60mV/dec so the supply voltage (VCC) scaling has slowed due to the leakage power budget and required minimum on-state drive current (Ion), which has fundamentally restrained the power consumption reduction for high-performance, low-power digital application. CMOS technology enforces challenges for ultra-low power analog/RF applications due the reduction of device intrinsic gain ($g_m/g_{ds}$) with technology scaling as well as the effective gain ($g_m/I_{ds}$) limit. Various innovations in devices have been investigated to improve the energy efficiency per computation for post-CMOS circuit and architecture application. Steep switching Tunnel FETs (TFETs), alternative device architecture, can enable further scaling of $V_{CC}$ for ultra-low power applications. III–V heterojunction TFET fig.9 have shown significant performance and power reduction in digital and for ultra low power analog/RF designs.

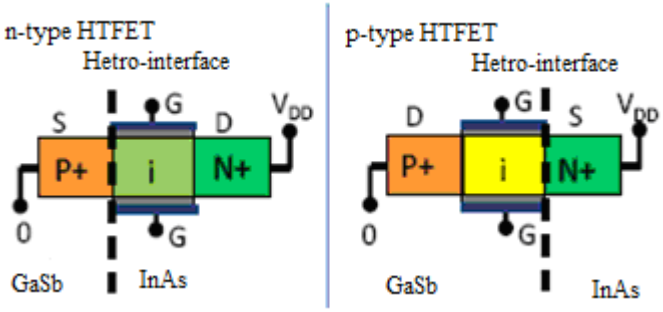



Fig.9 Hetrojunction TFET. From [29]

### A. *High Effective Gain $g_m/I_{DS}$ due to Steep Switching*

$g_m/I_{DS}$ metric as the effective gain per energy step is the key factor for low power analog circuit design. In MOSFETs, the peak $g_m/I_{DS}$ is achieved at the device sub-$V_{TH}$ region:

$$g_m = \frac{I_{D0}}{nV_t}\exp\left(\left(\frac{V_{GS}-V_T}{nV_t}\right)\left(1-\exp\left(-\frac{V_{DS}}{V_t}\right)\right)\right) \tag{8}$$

$$\frac{g_m}{I_{DS}} \approx \frac{1}{nV_t} < \frac{1}{26mV} = 40V^{-1}$$

Since MOSFET sub- $V_{TH}$ current follows kT/q slope, $g_m/I_{DS}$ has an upper limit of 40 $V^{-1}$ at 300K. In steep switching devices, $g_m/I_{DS}$ can overcome the 40 $V^{-1}$ limit:

$$\frac{g_m}{I_{DS}} = \frac{\partial I_{DS}}{\partial V_{GS}}\frac{1}{I_{DS}} = \frac{\partial \ln I_{DS}}{\partial V_{GS}} = \frac{\ln 10 \partial \log I_{DS}}{\partial V_{GS}} = \frac{\ln 10}{S} \tag{9}$$

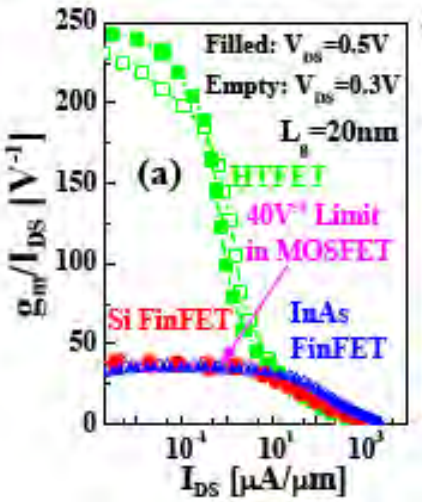



Fig.10 Comparison of $g_m/I_{DS}$ Vs. $I_{DS}$ for HTFETs, III-V and Si FinFETs. From [30]

Fig.10 shows the $g_m/I_{DS}$ Vs. $I_{DS}$ comparison for HTFETs, III-V and Si FinFETs, where HTFETs show improved gm/IDS at low IDS. This shows that HTFET is widely used for low-power analog application.

*B. Energy Versus Performance*

CMOS technologies do not offer much design space in the sub 0.5 V operating regime, because of their limited subthreshold swings. A new class of tunneling devices have been proposed[32] to minimize active and leakage power by scaling down the supply voltage below 0.5 with acceptable operating frequency in a few GHz range. In conventional tunnel field effect transistor (TFET) devices, tunneling takes place within 1–2 nm ($T_{TUN}$) of inversion layer; however, the fundamental bottleneck is that $T_{TUN}$ cannot be increased significantly by changing technology or process parameters, so drive current is limited by tunneling area ($W \times T_{TUN}$), $W$ being the device width. Area tunneling FET device resolve this problem by allowing tunneling across a wider area under the gate and the tunneling cross section is given by ($W \times L_G$). Fig. 11 shows the cross sectional diagram of conventional or width scaled TFET and nonconventional or area scaled TFET

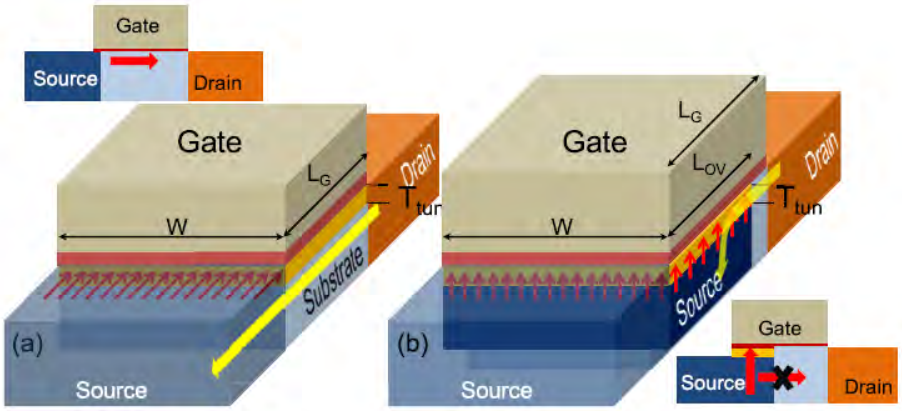



Fig.11 Cross sectional diagram of (a) conventional or width scaled TFET and (b) nonconventional or area scaled TFET. From[31]

A longer battery life is essential for handheld and mobile applications in idle state, which is governed by energy consumption in the device. Due to this reason, static energy ($P_{st} \times \tau$ ) is as a function of maximum operating frequency ($\tau$−1) is shown in Fig. 12, where $\tau$ being the stage delay . It shows that A MOS-HP dissipates more energy in idle state than the rest of the devices. This becomes worse at low operating frequencies making these devices unsuitable for applications where high battery life is required in idle state. The reason for this behaviour is that all devices except MOS-HP have got a very low leakage. Therefore, at a lower operating frequency and for a fixed $V_{DD}$, it is important to optimize the device for a lower leakage current.

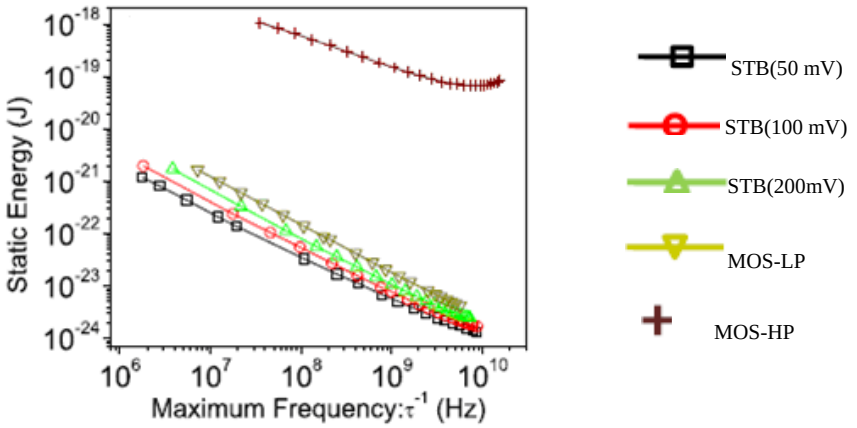



Fig. 12.Static Energy Vs. Maximum Operating Frequency. From [32]

The total energy per operation as a function of performance (operating frequencies) can be found using the following equation [32]

$$E_a = V^2_{DD} C L^2_d f^2 \left( \frac{\alpha}{2 L_d f} + \frac{I_{off}}{I_{on}} \right) \quad (10)$$

where $L_d$ = logic depth, $\alpha$ = activity factor, $C$ = Capacitance in $f_F$, and $f$ = fan out.

Some demanding applications on mobile devices require a sufficient level of performance. In all those applications, it is necessary to take the EDP into account for device assessment [32]. Due to higher energy and higher delay, the MOS-LP could not be used in such applications.

The reason for this behaviour is that, at reduced EOTs, gate control over epitaxial region improves, which enhances $I_{ON}$. This is manifested in a lower EDP product. MOS-LP devices require a higher *V*DD for achieving the targeted performance leading to overall higher energy dissipation per operation. A MOS-HP although uses a similar *V*DD as that of area scaled TFET, its higher static energy leads to an increased overall energy in the low to medium frequency region. Because of the relatively higher ON currents at lower supply voltages and a lower leakage current, STBFET consumes lesser energy for operating frequencies <4-GHz.

## VI. TFET FOR ENERGY EFFICIENT DIGITAL APPLICATIONS

CMOS technology has been an ideal framework to realize digital designs over the past four decades due to its desirable performance, power, cost and reliability characteristics. The continued scaling of the MOSFET device leads to an increased leakage (OFF state) current due to short channel effects such as Drain Induced Barrier Lowering (DIBL). The Tunnel FET demonstrated to possess more attractive operating characteristics when compared to CMOS at future technology nodes.

### *A. Dynamic Circuits utilizing only nTFETs*

In MOSFET based designs, only p-channel devices are employed as pull-up transistors since using a n-channel device results in a degradation of the output voltage levels equivalent to the threshold voltage of the device ($V_t$ drop). However, nTFETs do not exhibit a significant $V_t$ drop and hence, can be used in the pullup network without affecting the robustness of the circuit. This unique property of TFETs provides designers with the opportunity to attempt novel circuit designs utilizing only nTFETs. A dual clocked dynamic design is shown in Fig.13. Using only nTFETs necessitates that both the pre-charge and evaluation transistors in the circuit are driven by a logic-high gate voltage bias and hence, the use of a dual-clocked scheme is advocated. However, as with any pre-charge and evaluate design, there exists the possibility of output voltage degradation due to charge-sharing among internal nodes. Traditionally, this drawback is overcome by using a pull-up transistor with an inverter to form a level-restorer circuit However, in this design, a single nTFET is sufficient to implement level restoration as shown in Fig.13. This also improves the response of the level-restore circuitry and improves the energy-delay characteristics by eliminating the impact of the inverter.

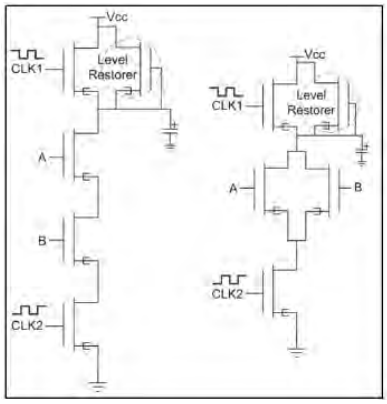
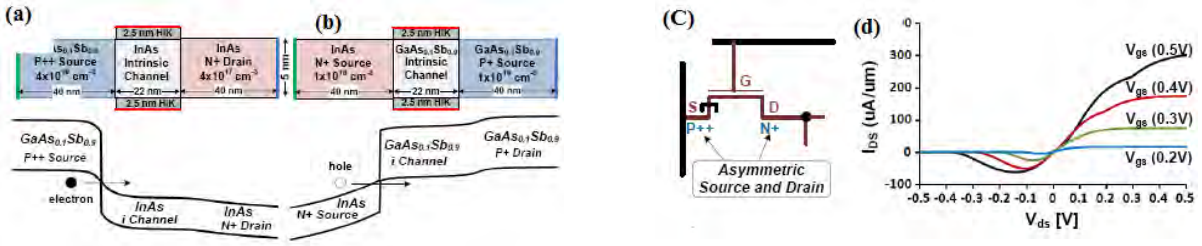



Fig.13. Dual-Clocked Dynamic NAND and NOR circuits employing only nTFETs. From [34]

### *B. Pass Transistor Logic for TFETs*

Pass Transistor Logic (PTL) designs use selection logic to enable or disable conduction paths between an input signal and the output. Although efficient in terms of latency and switching energy, a key feature of PTL designs is the requirement that all transistors be capable of conduction in either direction.



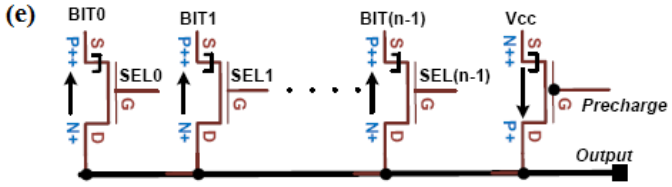



Fig. 14 (a) Double-Gate H-NTFET device structure and operation,(b) Double-Gate H-PTFET device structure and operation, (c) Asymmetric source-drain architecture for a heterojunction NTFET, (d) Asymmetric ID − VD characteristics resulting from source-drain asymmetry, (e) pass-transistor stack made of N-HTFETs, with a P-HTFET for precharging the output . From [32].

As previously noted, TFETs are predominantly unidirectional devices that exhibit asymmetric current conduction are not capable of satisfying this requirement without some additional design effort. It is also important to consider a solution for logic, because of the universal usage of pass transistors in logic design. A pass-transistor stack made of N-HTFETs, with a P-HTFET for precharging the output was proposed in Fig14.e.

All the N-HTFET transistors in the pass-transistor stack will be oriented toward the output which allows them to drive the On current when the input signals are enabled. During the pre-charge phase, the P-HTFET precharges the output to VCC, and during the evaluate phase, the N-HTFET stack evaluates the output based on the inputs to the pass-transistor stack.

C. *Bi-directional Switch based PTL*

Two nTFETs, with their drains oriented in opposite directions are used to create a bi-directional switch as shown in the Fig.15. It operates just like a NMOS pass transistor, the evident drawback of this implementation is that circuit area is doubled. Additionally, the range of operating voltages must be limited to ensure that no nTFETs in the PTL stack become significantly forward-biased, resulting in unwanted large conduction currents without regard to the gate voltage. A 4:1 multiplexer designed using these bi-directional switches is shown in inset of Fig 15.

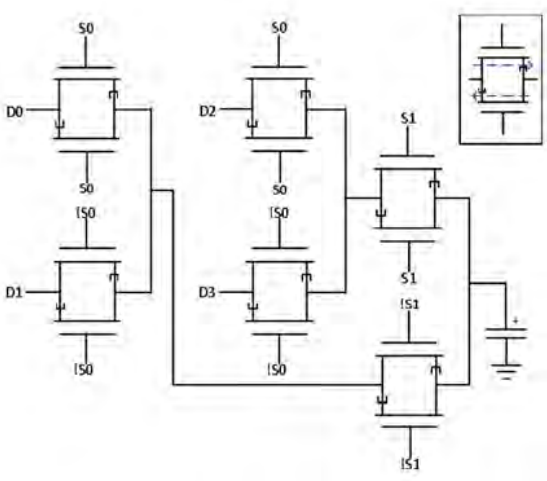



Fig.15. A 4:1 Multiplexer implemented using bi-directional switches. Direction of current flow through nTFETs in bi-directional switch shown in inset. From[34]

*2) Pre-charge Dynamic PTL:*

Dynamic pre-charge design is used as an alternative design to avoid doubling of area in bi-directional switch In this case, the TFETs in the pass transistor stack are oriented to only discharge the output node, which is precharged to V*cc* every cycle. The inputs of the PTL stack must be isolated from the output node while pre-charging to prevent the possibility of a direct V*cc* to GND shortcircuit. Fig 16 shows an area efficient implementation of 4:1 MUX using pre-charge based PTL.

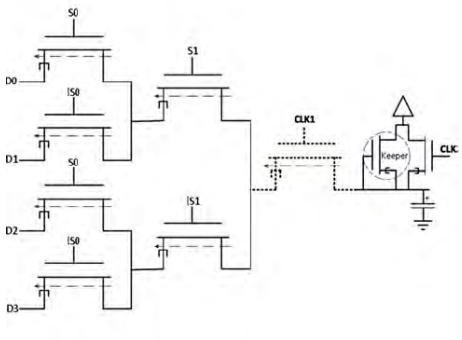



Fig.16. A 4:1 MUX implemented using Pre-Charge PTL. Direction of current flow is indicated by the dotted arrow. From[34]

The transistor shown with dotted lines is used to isolate the inputs during the pre-charge cycle. A nTFET based level-restorer circuit, as described above, is also added to negate the impact of charge sharing. The biggest advantage of this design is that only the internal capacitances on the path connecting the input to output in the stack are charged. This is unlike the static design, presented above, where some charged nodes may be charged needlessly. Despite these advantages, a subtle drawback inherent to this type of design is a limited range of operating voltages. As in the Bi-directional switch PTL, this is to prevent any nTFETs in the PTL stack from becoming significantly forward-biased.

## VII. CONCLUSION

The survey of TFET shows that steep subthreshold devices have advantages over conventional MOSFETs, such as lower subthreshold swing, temperature-independent $I_{OFF}$ and the potential to have much lower $I_{OFF}$ than the ITRS requirement without performance penalty. But TFET has low on-current ($I_{ON}$) compared to MOSFET, to enhance $I_{ON}$ some novel architecture are reviewed in this paper. It is reviewed that high on-currents $I_{ON}$ are predicted using narrow bandgap materials, heterojunction and dual material strained double gate structure. TFETs also provide additional performance benefits in terms of both energy and delay for logic designs. This paper clearly demonstrate that TFET devices are viable and attractive candidates for the future of digital logic designs, especially at ultra-low voltages. Due to the uni-directional conduction TFET based circuit design requires modification and optimization to achieve the optimal performance comparing to the traditional CMOS circuits. Variations and parasitic impact on the TFET circuit performance need to be addressed in future work.

## REFERENCES

[1] Mahdi Vadizadeh, Morteza Fathipour, Arash Amid "A Novel Nanoscale TFET Structure for increasing Ion/Ioff Current Ratio," 10th International Conference on Microelectronics, IEEE,pp. 300 -303,2008.

[2] Yasin Khatami, Kaustav Banerjee, "Steep Subthreshold Slope n- and p-Type Tunnel-FET Devices for Low-Power and Energy-Efficient Digital Circuits," IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 56, NO. 11, pp.2752- 2760, NOVEMBER 2009

[3] Ram Asra, Mayank Shrivastava, Kota V. R. M. Murali, Rajan K. Pandey, Harald Gossner, V. Ramgopal Rao, "A Tunnel FET for VDD Scaling Below 0.6V With a CMOS-Comparable Performance," IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 58, NO. 7,pp. 1855-1863, JULY 2011

[4] D. J. Wouters, J. P. Colinge, and H. E. Maes, "Subthreshold slope in thin-film SOI MOSFETs," IEEE Trans. Electron Devices, vol. 37, no. 9, pp. 2022–2033, Sep. 1990.

[5] H. C. Lin, M. H. Lee, C. J. Su, and S. W. Shen, "Fabrication and characterization of nanowire transistors with solid-phase crystallized poly-Si channels," IEEE Trans. Electron Devices, vol. 53, no. 10, pp. 2471–2477, Oct. 2006.

[6] K. Gopalakrishnan, P. B. Griffin, and J. D. Plummer, "I-MOS: A novel semiconductor device with a subthreshold slope lower than kT/q," in IEDM Tech. Dig., 2002, pp. 289–292.

[7] J. Appenzeller, Y.-M. Lin, J. Knoch, and P. Avouris, "Band-to-band tunneling in carbon nanotube field-effect transistors," Phys. Rev. Lett., vol. 93, no. 19, pp. 196 805-1–196 805-4, Nov. 2004.

[8] J. Knoch, S. Mantl, and J. Appenzeller, "Impact of the dimensionality on the performance of tunneling FETs: Bulk versus one-dimensional devices," Solid State Electron., vol. 51, no. 4, pp. 572–578, Apr. 2007.

[9] H. C. Lin, M. H. Lee, C. J. Su, and S. W. Shen, "Fabrication and characterization of nanowire transistors with solid-phase crystallized poly-Si channels," IEEE Trans. Electron Devices, vol. 53, no. 10, pp. 2471–2477, Oct. 2006

[10] P.-F. Wang, K. Hilsenbeck, T. Nirschl, M. Oswald, C. Stepper, M. Weis, D. Schmitt-Landsiedel, and W. Hansch, "Complementary tunneling transistor for low power application," Solid State Electron., vol. 48, no. 12, pp. 2281–2286, Dec. 2004.

[11] K. Bhuwalka, M. Born, M. Schindler, M. Schmidt, T. Sulima, and I. Eisele, "P-channel tunnel field-effect transistors down to sub- 50 nm channel lengths," Jpn. J. Appl. Phys., vol. 45, no. 4B, pp. 3106–3109, Apr. 2006.

[12] T. Nirschl, S. Henzler, J. Fischer,M. Fukle, A. Bargagli-Stoffi , M. Sterkel, J. Sedlmeir, C. Weber, R. Heinrich, U. Schaper, J. Einfeld, R. Neubert, U. Feklmann, K. Stahrenberg, E. Ruderer, G. Georgakos. R. Kakoschke, W. Hansch, and D. Schmitt-Landsiedel, "Scaling properties of the tunneling fi eld effect transistor (TFET): Device and circuit," Solid State Electron., vol. 50, no. 1, pp. 44–51, Jan. 2006.

[13] Semiconductor Industry Association (SIA), International Technology Roadmap for Semiconductors (ITRS), 2005. [Online]. Available: http:// www.itrs.net/

[14] K.Boucart, A.Ionescu, "Double Gate Tunnel FET with high k Gate Dielectric," IEEE Transaction on Electron Devices Volume 54,Issue 7, July 2007, pp. 1725–1733.

[15] Nayan Patel, A.Ramesha ,Santanu Mahapatra,"Drive current boosting of n-type tunnel FET with strained SiGe layer at source,." Microelectronics Journal Volume 39 ,2008, pp. 1671–1677.
[16] J. Knoch, J. Appenzeller,," A novel concept for field effect transistors—the tunneling carbon nanotube FET," in: Proceedings of the 63rd DRC, vol. 1, June 20–22, 2005, pp. 153–158.
[17] K. Bhuwalka,J. Shulze, "A simulation approach to optimize electrical parameters of a vertical tunnel FET," IEEE Trans. Electron Devices 52 (7) (2005) 1541–1547
[18] Kathy Boucart, Adrian Mihai Ionescu, "Double Gate Tunnel FET with ultrathin silicon body and high-k gate dielectric," in Proc. ESSDERC,2006,pp.383-386.
[19] Chen Shen, Li-Tao Yang, Ganesh Samudra, Yee-Chia Yeo, "A new robust non-local algorithm for band-to-band tunneling simulation and its application to Tunnel-FET," Solid-State Electronics 57 (2011) 23–30
[20] S.M. Sze, Physics of Semiconductor Devices, 2nd edn (New York: John Wiley & Sons, Inc., 1981)
[21] Sneh Saurabh , M. Jagadesh Kumar , "Novel Attributes of a Dual Material Gate Nanoscale Tunnel Field-Effect Transistor," IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 58, NO. 2, FEBRUARY 2011, pp 404-410.
[22] Min-Chul Sun, Sang Wan Kim, Garam Kim, Hyun Woo Kim, Jong-Ho Lee, Hyungcheol Shin, and Byung-Gook Park , "Scalable Embedded Ge-Junction Vertical-Channel Tunneling Field-Effect Transistor for Low-Voltage Operation," in Proc IEEE Nanotechnology Materials and Devices Conference 2010, pp. 286-290.
[23] V. Nagavarapu, R. Jhaveri, and J. C. S. Woo, "The Tunnel source (PNPN) n-MOSFET: A novel high performance transistor," IEEE Trans. Electron Devices, vol. 55, no. 4, pp. 1013–1019, Apr. 2008.
[24] Sayani Ghosh and Chandan K.Sarkar, "A Subthreshold Surface Potential Model to Study the effect of Dual Material Gate in Gate All Around n-TFETs," in Proc. CODIS 2012, pp 153-156.
[25] F. Mayer, C. Le Royer, J.-F. Damlencourt, K. Romanjek, F. Andrieu, C. Tabone, et al., "Impact of SOI, Si1−xGexOI and GeOI substrates on CMOS compatible tunnel FET performance," in Proc. IEEE IEDM, Dec. 2008, pp. 163–166.
[26] D. Leonelli, A. Vandooren, R. Rooyackers, A. S. Verhulst, S. D. Gendt, M. M. Heyns, et al., "Silicide engineering to boost Si tunnel transistor drive current," . J. Appl. Phys., vol. 50, no. 4, pp. 04DC05-1–04DC05-4, 2010.
[27] K. Jeon, W.-Y. Loh, P. Patel, C. Y. Kang, J. Oh, A. Bowonder, et al., "Si tunnel transistors with a novel silicided source and 46 mV/dec swing," in Proc. Symp. VLSI Technol., Jun. 2010, pp. 121–122.
[28] L. Knoll, Q.-T. Zhao, A. Nichau, S. Trellenkamp, S. Richter, A. Schäfer, et al., "Inverters with strained Si nanowire complementary tunnel field-effect transistors," IEEE Electron Device Lett., vol. 34, no. 6, pp. 812–815, Jun. 2013.
[29] Huichu Liu1, Ramesh Vaddi, Suman Datta and Vijaykrishnan Narayanan, "Tunnel FET-based Ultra-Low Power, High-Sensitivity UHF RFID Rectifier, " Proc. in Symposium on Low Power Electronics and Design , 2013, pp 157-162
[30] R. Asra, M. Shrivastava, K. V. R. M. Murali, R. K. Pandey, H. Gossner, and V. Ramgopal Rao, "A tunnel FET for VDD scaling below 0.6 V with a CMOS-comparable performance," IEEE Trans. Electron Devices, vol. 58, no. 7, Jul. 2011.pp. 1855–1863.
[31] S. Hanson, B. Zhai, K. Bernstein, D. Blaauw, A. Bryant, L. Chang, K. K. Das, W. Haensch, E. J. Nowak, and D. M. Sylvester, "Ultra low voltage minimum-energy CMOS," IBM J. Res. Develop., vol. 50, nos. 4–5, pp. 469–490, Jul. 2006.
[32] Anukool Rajoriya, Mayank Shrivastava, Harald Gossner, Thomas Schulz, and V. Ramgopal Rao, " Sub 0.5 V Operation of Performance Driven Mobile Systems Based on Area Scaled Tunnel FET Devices," IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 60, NO. 8, AUGUST 2013. pp 2626 – 2633.
[33] Vinay Saripalli, Asit Mishra, Suman Datta and Vijaykrishnan Narayanan, "An Energy-Efficient Heterogeneous CMP based on Hybrid TFET-CMOS Cores," DAC 2011, June 5-10, 2011. pp 729-734.
[34] Ravindhiran Mukundrajan, Matthew Cotter, Sungmin Bae, Vinay Saripalli, Mary Jane Irwin, Suman Datta, Vijaykrishnan Narayanan, "Design of energy-efficient circuits and systems using tunnel field effect transistors," IET Circuits Devices Syst., 2013, Vol. 7, Iss. 5, pp. 294–303