Delta- Sigma Modulator based Discrete Data Multiplier with Digital Output

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Abstract—In the proposed multiplier configuration, a new technique is proposed for multiplication of two sampled analog signals and the output is in digital form. One analog signal is fed to the input of first delta-sigma modulator (DSM1) after sampling. The sampled output of the second analog signal is negated or not negated depending on the bit state at the output of DSM1 and is fed to the input of second DSM(DSM2).The resulting bit stream at the output of DSM2 is the digital representation of the product of the sampled data of the two analog signals.

I. INRODUCTION

The second order, single stage, discrete, single bit quantizer and unity feedback gain Delta-Sigma Modulator (DSM) [1],[2] is shown in Fig. (1), and is a typical DSM where x_{analog} is the analog input signal. The Sample and Hold (S/H) circuit over samples the input signal at a sampling period (update period) T_U. The DSM circuit is operated by the clock with period T_C ($T_C << T_U$). *x(i)* is the sampled analog input signal to the DSM circuit during the i^{th} sampling period. *x1(i,j), x2(i,j), z(i,j)* and *e(i,j)* represents the first integrator output, second integrator output, quantizer output and quantizer error signal in i^{th} sampling period and during j^{th} clock period. The average values of the outputs of the first integrator, second integrator, quantizer and error signal during i^{th} update period are denoted as *x1(i), x2(i), z(i)* and *e(i)* respectively. The block D is the delay unit of one clock period. The normalized input signal during the i^{th} update period, *xnor(i)*, is the ratio of *x(i)* to the feedback gain.

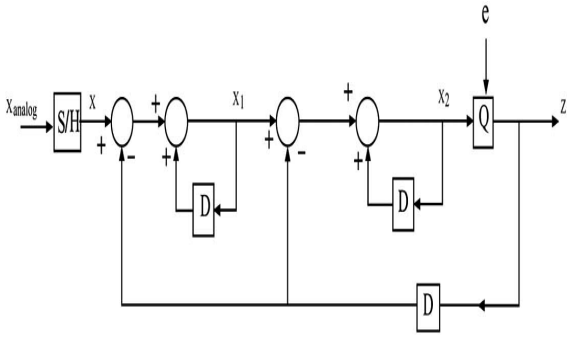

Fig. 1. Schematic diagram of typical second order DSM.

For a typical DSM with unity feedback gain, *z(i)* is equal to *x(i)*during the i^{th} update period. The subscript *i* is dropped in the figures and in further discussion. If the quantizer output is + V_S then the range of x_{analog} is $-0.7V_S < x_{analog} < +0.7V_S$. Input signal dependant feedback gain and input signal dependant operating period is used in DSM, to make the DSM more stable for extended range of input and suitable for industrial applications [3]. In the patents [4] and [5] and in the papers [6] and [9], the accuracy of, analog multipliers which use different techniques, is limited by the tolerance of the analog components. In [4] an analog multiplier which comprises a pair of differential cells, each cell comprising a pair of bipolar transistors with coupled emitters is presented for very low supply voltage with less distortion at the output of multiplier. In [5] is discussed an analog multiplier which has MOS input stage which provides good linearity range for the multiplier.

In [6] is proposed a four quadrant CMOS multiplier in which the output voltage swings with linearity of less than 1%. The dynamic ranges of the two input signals are 72% and 48% of supply voltage, + 2.5V. In [7] are compared eight categories of transconductance multipliers. The best linearity out of the eight categories of multipliers is about 0.5%. The low cost precision multiplier which is supplied by Analog Devices has maximum four quadrant accuracy of 2% of full scale [8].

The analog multiplier which is proposed in [9] is used for power and energy measurement and the power is measured with an accuracy of ±0.25%. In [10] is proposed cmos four quadrant analog multiplier which gives better bandwidth and less power dissipation but accuracy is not improved. In [11] is proposed analog multiplier using operational amplifiers and the linearity error in the multiplier is 0.09%.

Zhangcai Huang *et. al.* proposed a four quadrant CMOS multiplier in which the output voltage swings with linearity less than 1%. The dynamic ranges of the two input signals are 72% and 48% of supply voltage [12]. Dei M. *et. al.* proposed Gilbert like CMOS multiplier based on linear current divider in which the distortion is less than 1% [13]. Han G. *et. al.* proposed eight categories of trans-conductance multipliers and compared. The best linearity out of the eight categories of multipliers is about 0.5% [14].

In the case of proposed DSM based multiplier, two DSMs working with same clock frequency multiply the two analog input signals and the result is in digital form. The tolerance requirements of analog components in the DSMs are relaxed. The cost paid for high accuracy is faster operation and is feasible as on-chip VLSI implementation technology advances. The proposed multiplier is DSM based four-quadrant multiplier with new technique. It has maximum accuracy of ±0.0344% of FS for low frequency signals when the sampling period of analog signals is 0.01sec and the DSMs operating clock period is 0.1μsec. The maximum value of the input signal can be increased to ±70% of feedback gain. The proposed multiplier has better accuracy and wider input range compared to the conventional CMOS multipliers. The major advantage is that it multiplies two low frequency analog signals and provides digital output directly which is useful for power electronics applications like motor control using SCs.

In this paper, the proposed low cost four quadrant multiplier uses a new technique using basically two typical DSMs, a switch and a NOT circuit. The standard available CMOS operational amplifiers' specification with DC gain (*Aod*) = 100V/mV, bandwidth = 10MHz, input offset voltage = 20μV and supply voltage = + 2.5V is considered for op-amps in this proposal. With considered specification of the CMOS op-amp., the proposed multiplier has maximum overall accuracy of + 0.46% of FS (full scale of supply voltage) for low frequency signals. The maximum value of the input voltages can be + 70% of the supply voltage because only dc signals are fed to DSMs. The input voltages of DSMs are restricted to 70% due to stability reasons. If + 2.5V is the supply voltage of the operational amplifiers used in the circuit then the input signals can range from -1.75V to +1.75V with feedback gain constant equal to 2.5. The proposed multiplier has better accuracy and wider input range compared to the conventional CMOS multipliers.

II. PROPOSED MULTIPLIER CONFIGURATION

The details of proposed multiplier including the block diagram, relation between inputs and output, accuracy of inverting amplifier, implementation of non-ideality factors and the advantages are presented in this section inverter circuit and the specification of op-amp which is used in the circuits.

A. Block Diagram of Proposed Multiplier

In this multiplier configuration a new technique is proposed for multiplication of two sampled discrete analog signals and the output is in digital form. One analog signal is fed to the input of first DSM (DSM1) after sampling. The sampled output of the second analog signal is negated or not negated depending on the bit state at the output of DSM1 and is fed to the input of second DSM (DSM2). The resulting bit stream at the output of second DSM is the digital representation of the product of the two analog signals.

The block diagram of the proposed multiplier is shown in Fig.2. The sample and hold circuit S/H1 samples the input signal x_{analog} at a sampling period T_U. The sampled analog input signal x is fed to the input of DSM1. The DSM1circuit is operating with the clock of period T_C ($T_U >> T_C$). The SR flip-flop is reset (phase Φ_{off}) during each positive transition of the clock signal. The output of the single bit quantizer, Q_1 is in 1 state or in 0 state. When the quantizer output is in 1 state, SR flip-flop is set (phase Φ_{on}).

The S/H2 circuit samples the input signal y_{analog} at a sampling period T_U. The DSM2 circuit is also operating with the clock of period T_C. The sampled analog input signal y is fed to the input of DSM2 during phase Φ_{on}. The variable y is negated and fed to DSM2 during phase Φ_{off}.

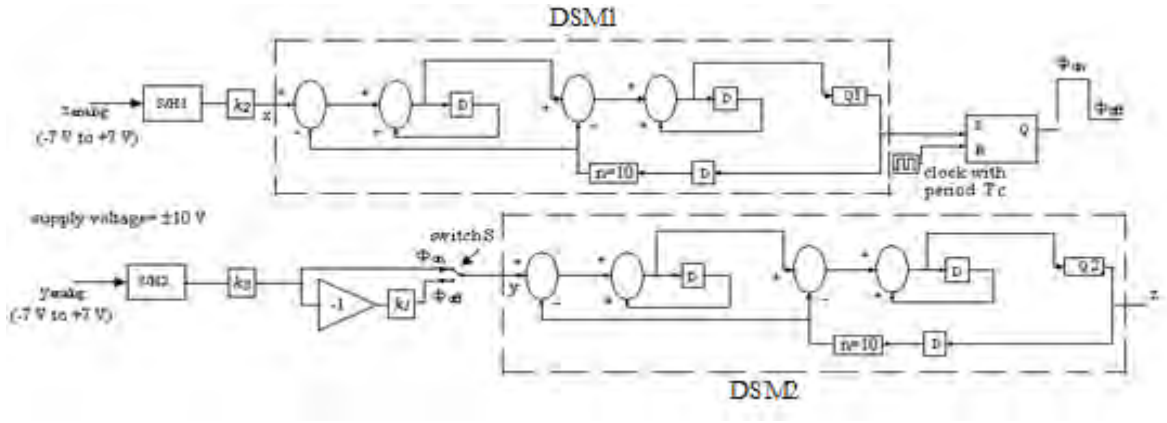

Fig. 2. Proposed Multiplier of Configuration

During each sampling period, the bit stream at the output of quantizer Q_2, gives the digital representation of the product of sampled input signals. The average value of the bit stream at the output during each sampling period (z) gives the analog value of the product of normalized samples of input signals $\left(\frac{x}{n}\frac{y}{n}\right)$. Therefore, the normalized value of *z* (*nz*) is equal to the normalized product of input signals $\left(\frac{xy}{n}\right)$. The resolution of DSM output Δz is given by, $\Delta z = \frac{T_C}{T_U} n$. However, Δz is limited by the realization of inverter circuit and the specification of op-amp which is used in the circuits.

B. Relation between Inputs and Output

Let *x,y* be the samples fed to DSM1 and DSM2 respectively in i^{th} sampling period. If $b_1, b_2 \ldots b_n$ are the stream of outputs of DSM1 during i^{th} sampling period, then the average analog input to DSM2 during T_U is given by $y(b_1 + b_2 + ... + b_n)\frac{T_C}{T_U}$ where $(b_1 + b_2 + ... + b_n)\frac{T_C}{T_U}$ is the normalized value of the input of DSM1 and is equal to *x/n*. Therefore,

$$y(b_1 + b_2 + ... + b_n)\frac{T_C}{T_U} = y\frac{x}{n} \tag{1}$$

The average value of bit stream at the output of DSM2, *z* is equal to the normalized value of input. Therefore,

$$z = \frac{x}{n}\frac{y}{n} \tag{2}$$

From equation (2), it can be stated that the average value of the digital output of the multiplier is equal to the product of the normalized samples of input signals.

C. Accuracy of Inverting Amplifier

The closed loop gain of the conventional inverting amplifier is given by,

$$A_V = \frac{V_{out}}{V_{in}} = -\frac{R_f}{R_i} \quad \frac{1}{\left(1 + \frac{1}{A_{od}}\left(1 + \frac{R_f}{R_i}\right)\right)} \tag{3}$$

where R_i and R_f are the input resistor and feedback resistor respectively. A_{od} is the open loop differential voltage gain of the operational amplifier. For unity gain inverting amplifier R_f and R_i should be equal. Substituting $R_f = R_i$ in equation (3), the closed loop gain of the unity gain inverting amplifier is given by,

$$A_V = \frac{V_{out}}{V_{in}} = - \frac{1}{\left(1+\frac{2}{A_{od}}\right)} \quad (4)$$

If $|V_{in}| = |(V_{out})_{ideal}|$, then $|V_{out}|$ represents the modulus of actual value obtained from the circuit. The equation (4) can be rewritten as

$$|V_{out}| = \frac{|(V_{out})_{ideal}|}{\left(1+\frac{2}{A_{od}}\right)} \quad (5)$$

The accuracy, γ is given by,

$$\gamma = \frac{|(V_{out})_{ideal}| - \frac{|(V_{out})_{ideal}|}{1+\frac{2}{A_{od}}}}{|(V_{out})_{ideal}|} \quad \ldots\ldots \quad \ldots..(6)$$

Using equations (5) and (6)

$$\%\gamma = \frac{\left(\frac{2}{A_{od}}\right)}{\left(1+\frac{2}{A_{od}}\right)} \times 100 \quad (7)$$

If A_{od} = 100V/mV, then the accuracy of inverter circuit is approximately 0.002%.

D. Implementation of Non-Ideality Factors in Simulation

To be more practical, A_{od} is considered to be 70 dB and the offset voltage is considered to be 5mV. With A_{od}=70dB, the accuracy of inverter circuit is 0.6mV. Considering the resolution as 5mV, if T_U = 0.01sec and n=10 then from equation $\Delta z = \frac{T_C}{T_U} n$, T_C can take a minimum value of 5μsec By selecting the resolution more than the specified input offset voltage there will not be any error due to the offset voltage in the inverter circuit.

Substituting A_{od}=3160 (70dB) in equation (8),

$$|V_{out}| = 0.99937 |(V_{out})_{ideal}| \ldots\ldots \quad \ldots..(8)$$

Therefore, the error due to the finite gain of the op-amp, which is used in the inverting amplifier, is included in the MATLAB model by inserting a gain element *k1* of value 0.99937 after inverter block.

The error due to the finite gain of operational amplifiers used in S/H1 and S/H2 and also the error due to the gain mismatch are considered. Nowadays, the best accuracy of S/H is about 14 bits. If the gain of S/H1 is 1+*a* then the gain of S/H2 is 1-*a* where *a* is the accuracy error and is equal to $1/2^{14}$. Therefore,

$$x = \left(1+\frac{1}{2^{14}}\right) x_{ana\log} = 1.000061 x_{ana\log} \quad (9)$$

$$y = \left(1-\frac{1}{2^{14}}\right) y_{ana\log} = 0.999939 y_{ana\log} \quad (10)$$

The error due to the finite gain of the op-amp, which is used in S/H1 and S/H2 circuits, is included in the MATLAB model by inserting, gain element *k2* of value 1.000061 after S/H1 block and gain element *k3* of value 0.999939 after S/H2 block. The accuracy requirements of analog components used in DSM are relaxed due to faster operation and correction through feedback.

III. SIMULATION RESULTS OF PROPOSED MUL2

The proposed DSM based multiplier is simulated with T_U =0.01 sec and T_C = 0.1μsec with ideal conditions (without including non-ideality factors). In Fig.3, the first waveform shows the sine signal of peak amplitude 7V and frequency 1 Hz (*x*) which is the multiplicand signal. The second waveform of Fig.3 shows the

sine signal of peak amplitude 7V and frequency 0.1 Hz (*y*) which is the multiplier signal. The ideal product (normalized to FS) of the two analog signals and the average value (normalized to FS) of the bit stream at the output of the proposed multiplier in each sampling period are shown in the waveforms (c) and (d). It can be seen from (d) that the normalized analog signal at the output of the proposed multiplier closely follows the normalized ideal product value. The waveform (c) shows the normalized product value after a delay of T_U. The error signal ((c)-(d)) is shown in the waveform (e). The absolute maximum value of the error signal is 0.344mV (0.0344%).

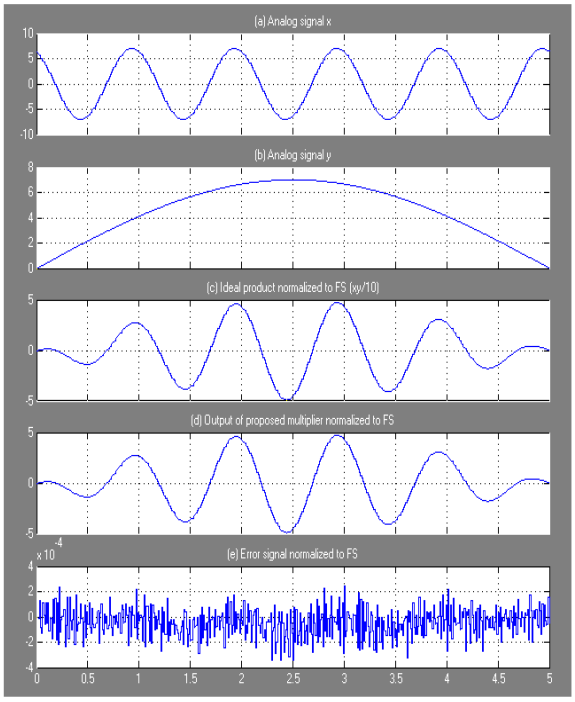

Fig. 3. Ideal Functioning of Proposed MUL2. (Horizontal axis-Time in sec, Vertical axis- Voltage in Volts, T_U =0.01 sec, T_C = 0.1µsec and n=10)

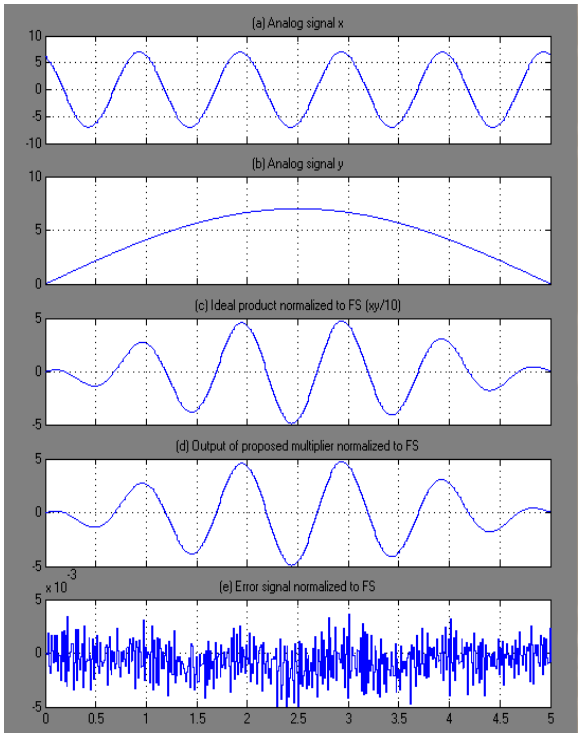

Fig. 4. Ideal Functioning of Proposed MUL2. (Horizontal axis-Time in sec, Vertical axis- Voltage in Volts, T_U =0.01 sec, T_C = 0.1µsec and n=10)

The proposed DSM based multiplier is simulated with T_U =0.01 sec and T_C = 5μsec with non-ideality parameters which are detailed in section.2.4. and the outputs are shown in Fig.4. The absolute maximum value of the error signal is 5mV (0.05%) as shown in the waveform (e). The accuracy taking into account the non-ideality factors is better than the existing multipliers.

IV. CONCLUSION

Two second order DSMs are used for multiplication of two sampled analog signals and the result is in digital form. For considered two low frequency analog signals, the maximum overall accuracy is ±0.03% of FS. The dynamic range of both input signals are 90% of supply voltage. The proposed multiplier has better accuracy and dynamic range compared to conventional CMOS multipliers and additionally it multiplies two analog signals and provides directly digital output useful for industrial electronics applications like motor control using switching converter

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