Performance Analysis of a Low Power Low Noise 4 – 13 GHz Ultra Wideband LNA

J.Manjula [#1], Dr.S.Malarvizhi [#2]

[#] ECE Department, SRM University,
Kattangulathur, Tamil Nadu, India-603203
[1] jmanjulathiyagu@gmail.com
[2] malarvizhig@rediffmail.com

Abstract-A low power low noise ultra wideband LNA of 4 -13GHz is presented. It employs a series LC sections for input impedance matching, current reuse and noise cancellation technique to reduce the power consumption and noise. The designed LNA is implemented in standard 180nm CMOS technology using ADS tool. The designed LNA has a transfer gain of 21dB and noise figure of less than 3dB over the range of 4 -13 GHz band of frequencies with a power consumption of 18mW. It exhibits an input reflection co-efficient (S_{11}) of less than -14dB within the entire band of frequencies and its IIP3 is -6dBm at 3GHz. Low power, low noise with high gain over the wide band of 4 – 13 GHz make it suitable for wide band RF front end.

Keywords: Ultra wide band LNA, Input matching network, Cascode stage, Noise figure, Current reuse.

I. INTRODUCTION

Rapid growth of wireless market emerges various communication systems capable of supporting multiple bands of frequencies, demands wideband RF front end [1] for global roaming. It increases the requirement of integrated CMOS products for high performance RF front end circuits. Using CMOS process, the RF systems can be realized with low power consumption, high frequency range (GHz) and high reliability. The block diagram of the Wideband RF front end is shown in Fig. 1.

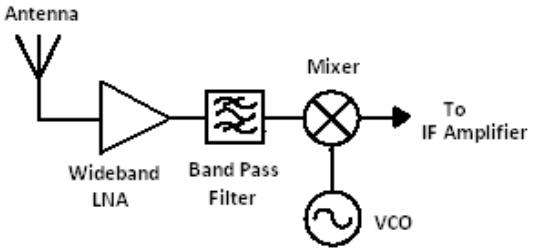

Fig. 1. Block Diagram of RF Front End

The Receiver RF front end has wideband low noise amplifier followed by band pass filter, mixer, VCO and so forth. The first stage of a receiver is typically a low noise amplifier (LNA), whose main function is to provide enough gain to overcome the noise of subsequent stages (such as a mixer) [2]. Main functions of LNA in a radiofrequency chain are both increasing signal energy and limiting noise in the receiver as much as possible. And also it demands low NF, sufficient gain with flatness over the wide frequency range, low power consumption and low cost. [3]. Block diagram of LNA of Fig. 2 has input/output matching networks with core amplifier design [4].

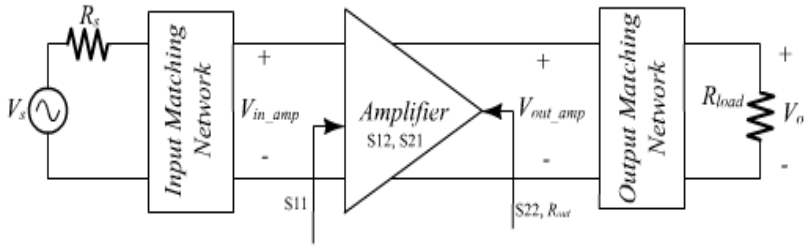

Fig. 2. Block Diagram of a LNA

Designing of wideband LNA is one of the challenging blocks in multi band receiver, with the designing issues of low noise characteristics over the band width, flat frequency response, input/output matching networks for maximum power transfer and stability [4] There are number of topologies are available for wide band matching [5 – 8], current reused technique [9, 12] and noise cancellation techniques [11] to improve the performance of wide band LNA. Common source stage with resistor shunt feedback technique [4], [6] is used to achieve broadband input matching, but it is difficult to achieve high power gain and low noise figure simultaneously. The common-gate LNA (CGLNA) topology [7] is more suitable for broadband input match; however, its noise figure is limited and consumes more power.

Cascode UWB LNA with transformer input matching network is discussed in [8]. Current reused two-stage LNA [9, 12], achieves low power consumption and sufficient gain with flatness but the noise figure is not satisfactory. A two-stage inverter-based LNA with three inductors reported in [10] achieves satisfied gain and NF but consumes high power of 18mW. All these approaches could not satisfy the required power gain, power consumption, and noise and linearity performance simultaneously.

This paper proposes ultra wide band LNA with series LC for input matching network with current reuse and noise cancellation techniques for low power and low noise. Section 2 and 3, describes the circuit operation and design of wideband LNA respectively. Discussion on simulation results and its layout are presented in section 4 and section 5 briefs the concluding remarks.

II. CIRCUIT DESCRIPTION ULTRA WIDEBAND LNA

The circuit schematic of Fig.3 is a two stage cascode wideband LNA with series connected L type LC sections for broad band input impedance matching. Cascode stages are preferred for high gain, high input/output impedance and large bandwidth with high voltage swing. The first cascode stage comprises M1 common source stage with inductive source degeneration (Ls) to exhibit good linearity and stabilize the amplifier for entire frequency range. Even though, it simplifies input impedance matching along with gate inductor Lg, it can achieve only narrow band matching. Thus, two series connected LC sections (C_1& L_1 and C_2 & L_2) have been used to match the input impedance of L-degenerated amplifier across a wide bandwidth. First L section (C_1& L_1) provides lower cutoff frequency and the second L section (C_2& L_2) provides upper cutoff frequency for broad band match. M_3 act as a common gate stage for cascode configuration to eliminate the miller effect and provides better isolation for output return signal.

The intermediate stage M_2 along with R_1, C_3 and L_5 forms a current reuse network where C_3 offers low impedance path and L_5 offers high impedance path for ac signal. Thus it reuses the charge stored across the capacitance C_3. The inductance L_5 increases the transconductance of common source stage (M_1) and also it provides good matching to feed the signal from M_1 to common gate stage (M_3). Further this design is robust against temperature and process variations [15].

The second cascode stage (CS stage (M_5) & CG stage (M_4)) is used to boost the gain and extend the band width with flatness. R_2 and R_5 are used for biasing the common source stages. For the purpose of shunt peaking at the high frequencies, the inductor loads L_3 and L_4 are used for the cascode stages. The inductive loads along with the drain parasitic capacitances of M_3 and M_4, provides gain roll at the high cut off frequencies of the band. Peaking inductor also features constant power gain over the entire bandwidth by compensating the decreasing impedance of capacitance with the increase of frequency [16].

Output buffer is a source follower which provides 50Ω wideband output matching for maximum power transfer. The major noise has been contributed by the common source stage of cascode networks. The noise at the drain of the common source stage M_7 is 180◦ out of phase with the noise at the source of common drain M_6. Thus the noise figure of the LNA has been reduced due the noise cancellation by M_7. As this design uses LC section wideband impedance matching networks with current reuse and noise cancellation techniques improve the performance of wideband LNA and make it more suitable for low power, low noise, and high gain wideband amplifier for RF front end.

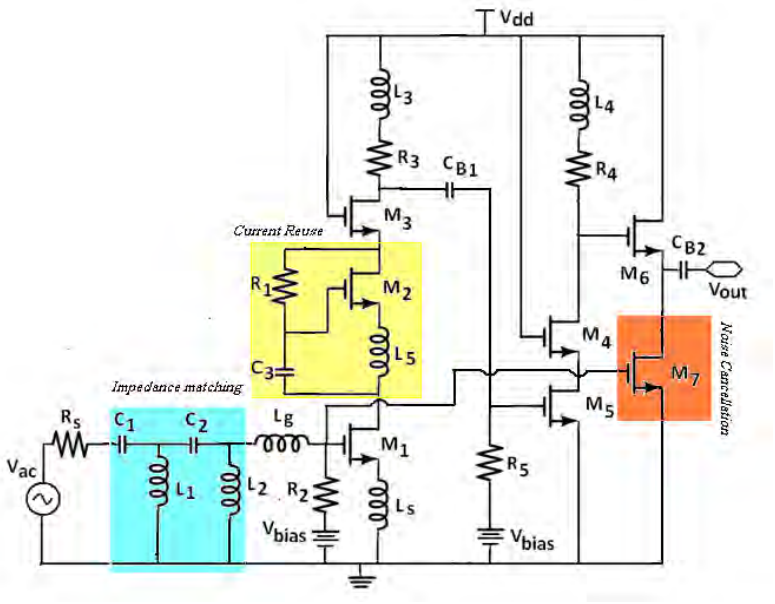

Fig. 3. Circuit Schematic of Proposed Wideband LNA

A. *Design of Wideband LNA*

1) Input wideband matching circuit

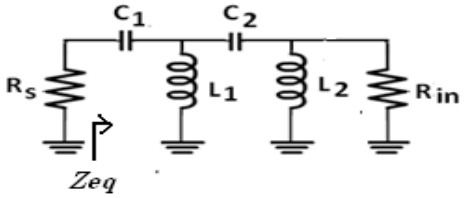

Fig. 4. Input Matching Network

For maximum power transfer, the input impedance of the amplifier has to be matched with the source impedance. Fig.4 shows the input matching network for the wideband LNA. R_s is the source resistance which is 50Ω has to matched with R_{in} of the amplifier for the entire band of frequencies. C_1L_1 and C_2L_2 are the two L sections used for wideband matching. The equivalent impedance Z_{eq} is calculated from the following Equation (1),

$$Z_{eq} = \left\{\left[\left(R_{in} \parallel jX_{L2}\right) + \left(-jX_{C2}\right)\right] \parallel jX_{L1}\right\} + \left(-jX_{C1}\right) \leftrightarrow (1)$$

The L sections are resonant at f_1 and f_2, which are given as,

$$X_{L2} = X_{C2}, \quad X_{L1} = X_{C1}$$

$$f_2 = \frac{1}{2\pi\sqrt{L_2C_2}} \qquad f_1 = \frac{1}{2\pi\sqrt{L_1C_1}}$$

At resonant frequencies the equivalent impedance is simplified as given in Equation (2),

$$Z_{eq} = \frac{R_{in} - j\left(X_{L1}R_{in}^2 - X_{L2} + X_{L2}^2X_{L1}\right)}{\left(1 - X_{L1}X_{L2}\right)^2 - \left(X_{L1}R_{in}\right)^2} \leftrightarrow (2)$$

The equivalent resistance of (3) is derived from the real part of equation (2),

$$R_{eq} = \frac{R_{in}}{\left(1 - X_{L1}X_{L2}\right)^2 - \left(X_{L1}R_{in}\right)^2} \leftrightarrow (3)$$

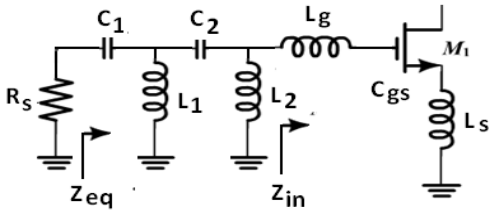

Fig. 5. Input impedance of LNA

The value of R_{in} is the real part of the input impedance of the LNA with degenerative inductance L_s and gate inductance L_g. The input impedance is calculated from the first stage of the LNA as in Figure 5 and is expressed as,

$$Z_{in} = \frac{L_s g_m}{C_{gs}} + j\left(\omega L_g - \frac{1}{\omega C_{gs}} + \omega L_s\right) \leftrightarrow (4)$$

The real part of the input impedance is given as,

$$R_{in} = \frac{L_s g_m}{C_{gs}}$$

By adjusting the values of L_1& L_2 of matching network and L_s, C_{gs} & g_m of M_1, the input impedance of wideband LNA can be matched with source resistance of 50Ω.

2) Gain of Wide band LNA

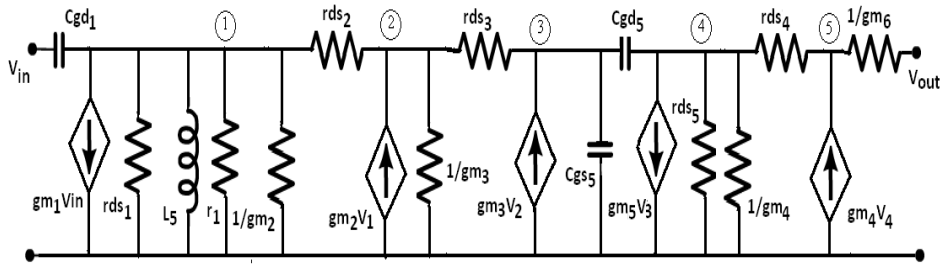

Fig. 6. Small Equivalent Circuit of Proposed Wideband LNA

The small equivalent circuit of wide band LNA (excluding input matching network) is shown in Fig.6. The voltage gain of the circuit is calculated using the equation (5) as given below.

$$A_v = \frac{V_{out}}{V_{in}} = \frac{\left(g_{m1} + g_{ds1} + g_1 + g_{m2} + g_{ds2} + \frac{1}{sL_5}\right)(g_{m3} + g_{ds3})(g_{m4} + g_{ds4})(sC_{gd5} + g_{m5})}{g_{ds2}\left[(g_{ds3} + C_{gs5} + C_{gd5})(sC_{gd5}g_{ds4} + g_{ds4}g_{ds5})(g_{m4} + g_{ds4}) + (g_{ds4}C_{gd5})(sC_{gd5} - g_{m5})\right]} \leftrightarrow (5)$$

Where g_m and g_{ds} are the transconductances of the stages. It is seen that the gain of the wideband LNA is proportional to the product of (g_{m1}+ g_{m2}), g_{m3}, g_{m4} and g_{m5}, hence the designed UWB LNA can attain high gain.

III. SIMULATION RESULTS AND DISCUSSION

The proposed wideband LNA has been designed and simulated in TSMC 0.18 μm CMOS technology using ADS tool. The performance of an amplifier is characterized by S parameters in terms of I/O reflection co-efficient (S_{11} and S_{22}), forward transfer gain (S_{21}) and reverse isolation (S_{12}) and noise figure.

A. Input / Output Reflection Co-efficient (S_{11} and S_{22}) and Reverse Isolation (S_{12})

For the proper impedance matching, the input and output reflection coefficients should be less than 10dB for the required band of frequencies. And also for the better reverse isolation S_{12} should be less than 50dB. The simulated results of Figures 7 & 8 have shown that S_{11} and S_{22} are less than -14dB and S_{12} ranges from 100dB to 80dB over the entire band of frequencies 4 -13GHz respectively.

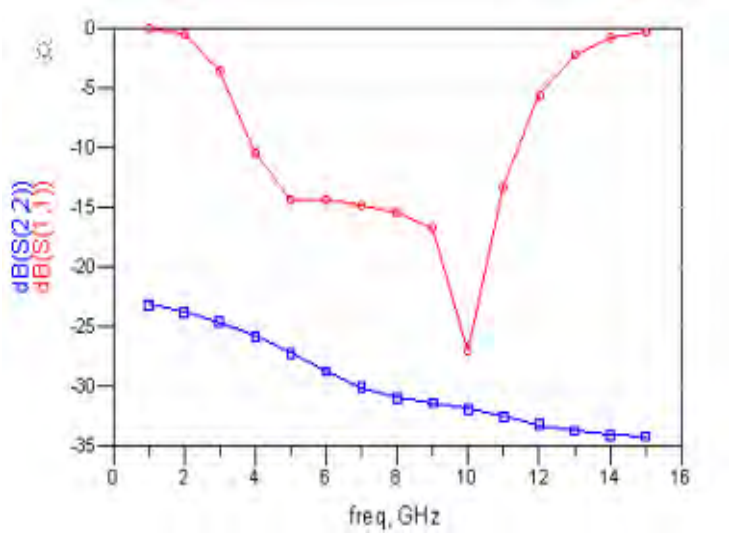

Fig.7 Input/Output Reflection Co-efficients (S_{11} and S_{22}) dB

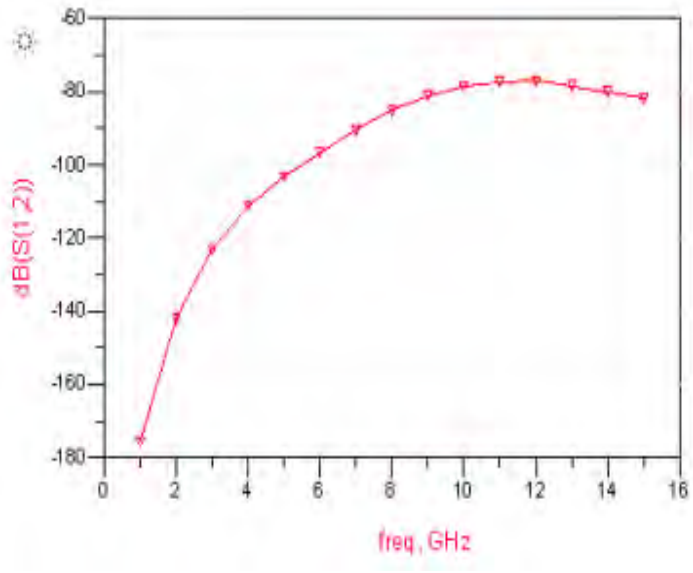

Fig.8 Reverse Isolation Loss (S_{12})dB

B. Forward Transfer gain (S_{21})

Two stages of cascode amplifier with wide band impedance matching have been used to achieve high gain over the wide band of frequencies 4 – 13 GHz. The simulation result of the Fig.9 has proved that the designed wide band LNA has a gain of more than 20dB for wide band. And also the use of current reused network reduces the power consumption to 18dB. Source inductive degeneration has made the circuit more stable with stability factor greater than or equal to one as shown in Fig.10.

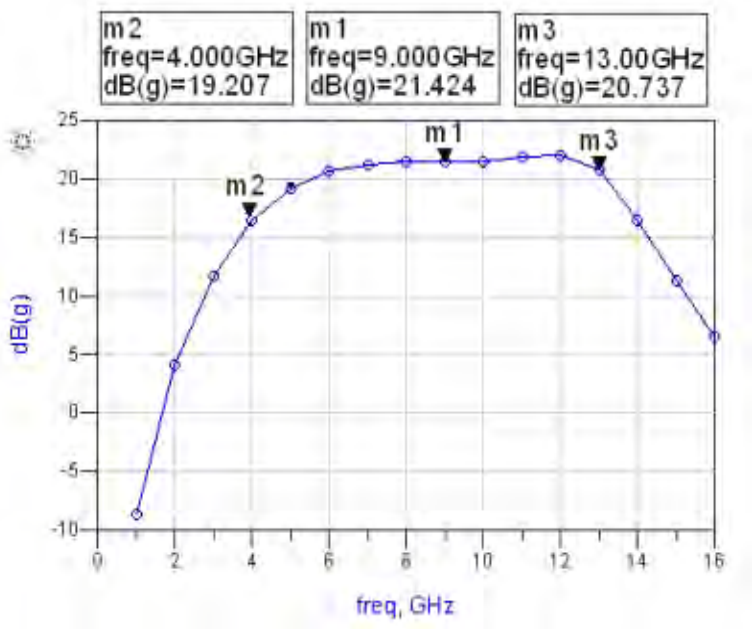

Fig.9 Frequency Response of Forward Transfer Gain (S_{21}) dB

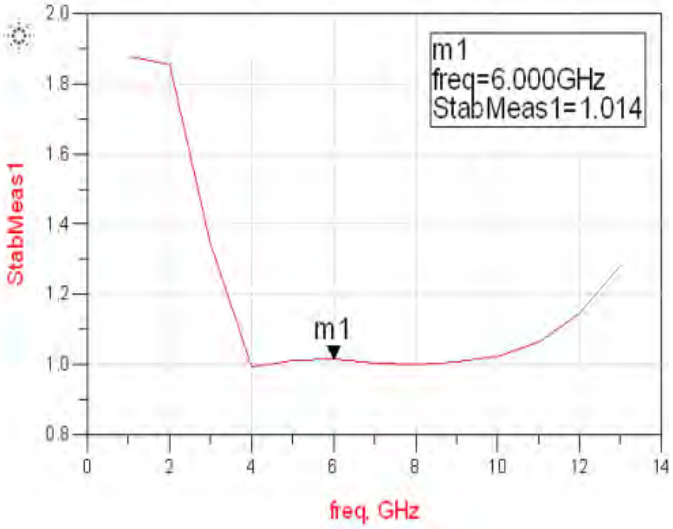

Fig.10 Stability Measure of LNA

C. Noise Figure

One of the design considerations of the wide band LNA is to maintain a low noise figure of less than 5dB for the entire band of frequencies. The noise contributed by M7 is out of phase with the noise contributed by M1, thus it reduces the noise figure over the designed band of frequencies. Fig. 11 shows the noise figure of the designed wide band LNA with and without noise cancellation techniques. The LNA with noise cancellation technique has reduced noise figure ranges from 1dB to 5dB for the designed wide band of 4 – 13GHz.

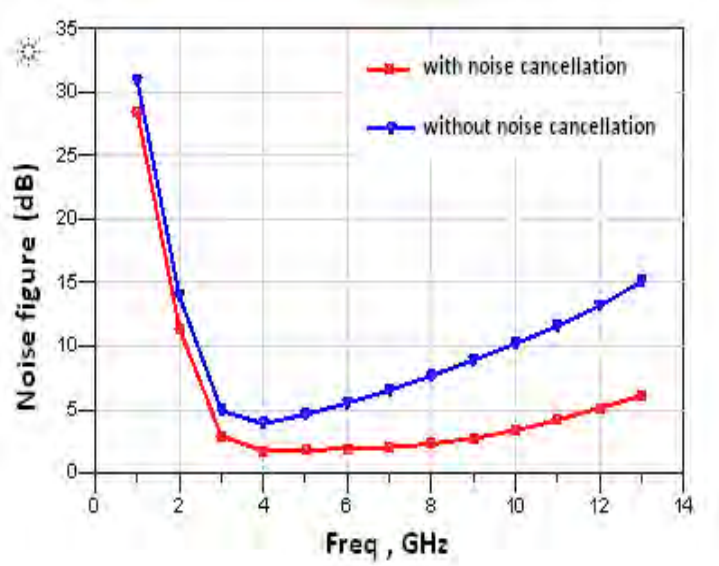

Fig.11 Noise Figure of LNA with and without Noise cancellation techniques

D. Linearity

The 1dB compression point of Fig.12 is obtained at the input power of -23dBm and the third order intercept point (IIP3) is -6dBm at 6GHz as shown in Fig.13. This is seen to be, the designed wide band LNA has better linear characteristics over the inter-modulation distortion.

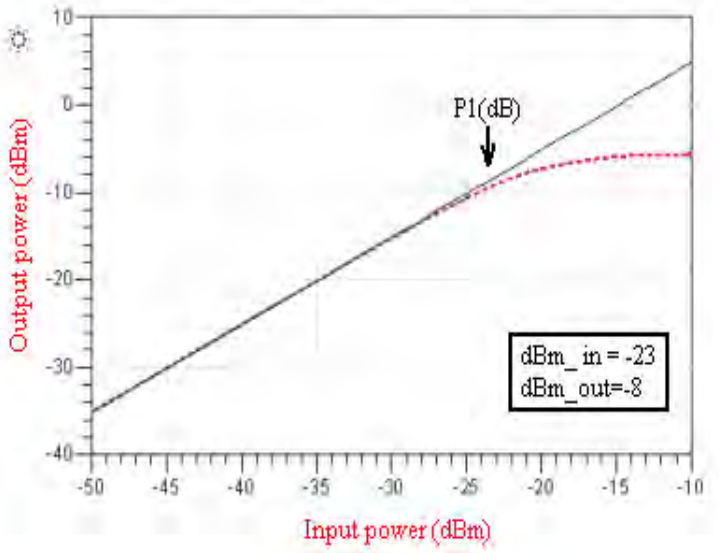

Fig.12 1dB Compression Point (P1dB)

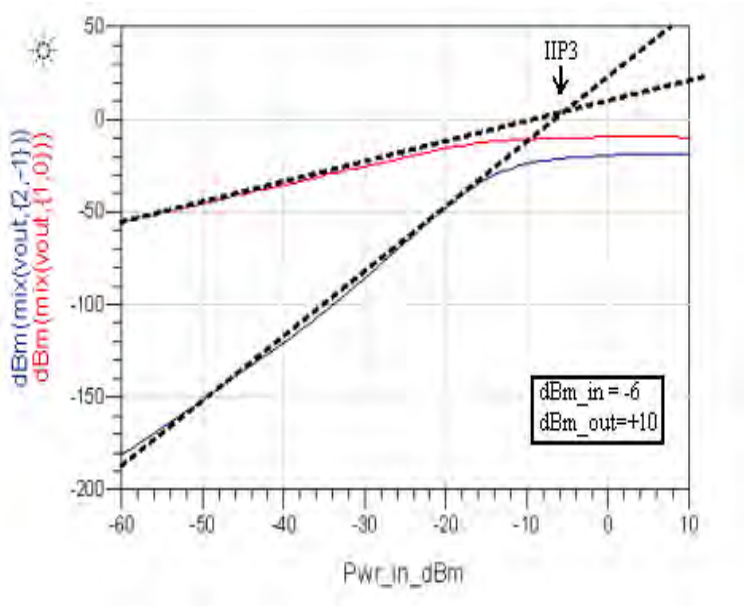

Fig.13 Third order Intercept point (IIP3)

E. Layout

The layout of the wideband LNA obtained from ADS layout tool is shown in Fig. 14.

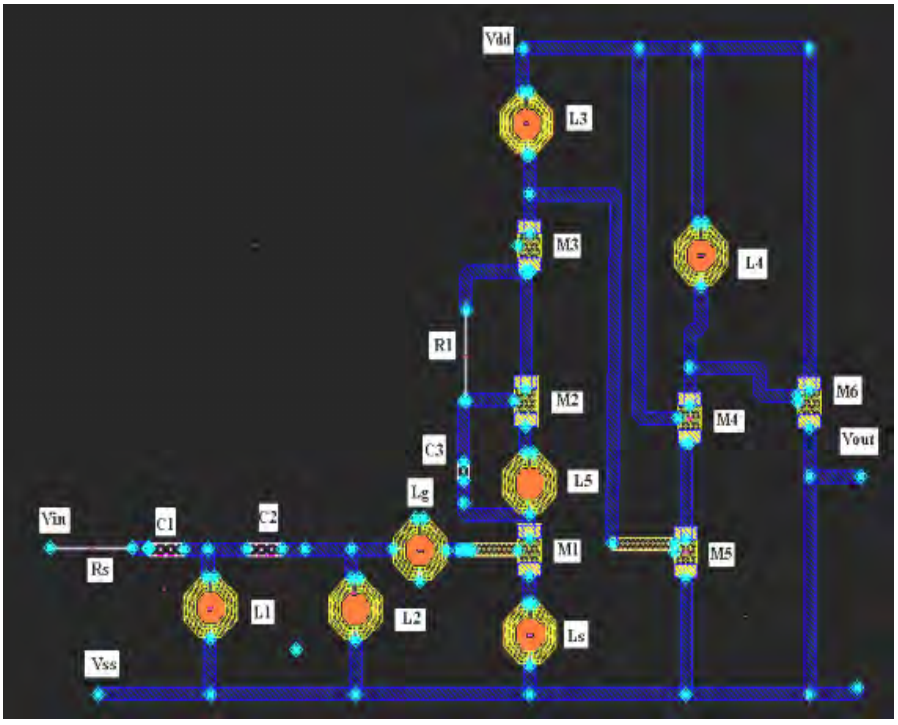

Fig. 14. Layout of Wideband LNA

F. Figure of Merit

To evaluate the performance of wideband LNA, a figure of merit (FOM) [14] is defined as equation (6). It is calculated to be 11.66.

$$\text{FOM [GHz/mW]} = \frac{(S_{21}.\text{Bw})}{[(\text{NF-1}).P_D]} \leftrightarrow (6)$$

IV. PERFORMANCE COMPARISON

Table 1 summarizes the performance comparison of the proposed wide band LNA with results of the references [10,15and17]. The comparison results prove that the designed LNA has high gain, low noise with good input impedance matching over the entire band of frequencies 4 – 13GHz.

TABLE 1
Performance Comparison of Wideband LNAs

Parameters	Ref [10]	Ref [15]	Ref [17]	This work
Technology	180nm	180nm	180nm	180nm
Band width (GHz)	3 - 10	3.1–10.6	1~5	4– 13
Gain (S21) dB	13.7±1.5	15.6	12.5~13	21
Input Return Loss (S11) dB	<-10.7	< –10	<-8	< -14
Power Consumption (mW)	18	14.1	18	18
Noise Figure (dB)	2.3±0.1	2.8–4.7	3.8	2
IIP3 (dBm)	-0.2	–7.1 @ 6GHz	-1 @ 3GHz	-6@ 3GHz
FOM(GHz/mW)	4.43	-	-	11.66

V. CONCLUSION

The design and performance analysis of 4 -13GHz ultra wide band LNA is demonstrated. It is simulated and implemented in 180nm CMOS technology using ADS tool. It has achieved high gain, low power and low noise with good input impedance matching over the entire band of frequencies which makes it suitable for wideband RF front end.

ACKNOWLEDGEMENT

The authors wish to thank ECE department of SRM University for supporting Agilent ADS tool sponsored by DST-FIST for this work.

REFERENCES

[1] Chao-Shiun Wang, Wei-Chang Li, and Chorng-Kuang Wang, “A Multi-Band Multi Standard RF Front end For IEEE 802.16a And IEEE 802.11A/B/G Applications”, IEEE International Symposium on Circuits and Systems (ISCAS, May 23-26, 2005.
[2] T. Lee, the Design of CMOS Radio-Frequency Integrated Circuits, Cambridge University Press, 1998.
[3] Bonghyuk park, Sangsung Choi, Sonhcheol Hong, “A Low-Noise amplifier with Tunable Interference Rejection for 3.1-10.6GHz UWB systems” IEEE Microwave And Wireless Components Letters, Vol.20, No.1, June 2010.
[4] Bosco Leung, Charles.G.Sodini, “VLSI for Wireless Communication”, Pearson Education, Edition 2009.
[5] Garuda, C et al. “A 3-5 GHz Fully Differential CMOS LNA with Dualgain mode for Wireless UWB Applications” IEEE Circuits and Systems 48th Midwest Symposium, Vol. 1 pp.790 – 793 Aug. 2005
[6] C.-W. Kim, M.-S. Kang, P. T. Anh, H.-T. Kim, and S.-G. Lee, “An ultra wideband CMOS low noise amplifier for 3–5 GHz UWB system,” IEEE J. Solid-State Circuits, vol. 40, no. 2, pp. 544–547, Feb. 2005.
[7] Y. Lu, K. Yeo, A. Cabuk, J. Ma, M. Do, and Z. Lu, “A novel CMOS low-noise amplifier design for 3.1- to 10.6-GHz ultra-wide-band wireless receivers,” IEEE Trans. Circuits Syst. I, vol. 53, no. 8, pp. 1683–1692, 2006.
[8] Dong Hun Shin, Jaejin Park, and C. Patrick Yue1, “A Low-Power, 3–5-GHz CMOS UWB LNA Using Transformer Matching Technique”, IEEE Asian Solid-State Circuits Conference, pp. 95 – 98, Nov 2007.
[9] G. Sapone and G. Palmisano, “A 3–10-GHz low-power CMOS lownoise amplifier for ultra-wideband communication,” IEEE Trans. Microw.Theory Tech., vol. 59, no. 3, pp. 678–686, Nov. 2011.
[10] Yo-Sheng Lin, Senior Member, IEEE, Chien-Chin Wang, Guan-Lin Lee, and Chih-Chung Chen, “High-Performance Wideband Low-Noise Amplifier Using Enhanced π -Match Input Network”, IEEE Microwave And Wireless Components Letters, 2013, (accepted for publication, This article has been accepted for inclusion in a future issue of this journal)}
[11] R. C. Liu et al., “Design and analysis of DC-to-14GHz and 22GHz CMOS cascade distributed amplifier,” IEEE J. Solid-State Circuits, vol. 39, pp. 1370-1374, Dec. 2004.
[12] Pou-Tou Sun, Shry-Sann Liao, Hung-Liang Lin, Chung-Fong Yang, and Yu-Hsuan Hsiao, “Design of 3.1 to 10.6GHz Ultra-wideband Low Noise Ampli¯er with Current Reuse Techniques and Low Power Consumption”, Progress In Electromagnetics Research Symposium, Beijing, China, March 23-27, 2009,pp. 901 – 905.
[13] Chang-Wan Kim, Min-Suk Kang, Phan Tuan Anh, Hoon-Tae Kim, and Sang-Gug Lee, “An Ultra-Wideband CMOS Low Noise Amplifier for 3–5-GHz UWB System”, IEEE Journal Of Solid-State Circuits, Vol. 40, No. 2, February 2005, Pp. 544 – 547.
[14] C. H. Wu, Y. S. Lin, J. H. Lee, and C. C. Wang, “A 2.87 0.19 dB NF 3.1–10.6 GHz ultra-wideband low-noise amplifier using 0.18 CMOS technology,” in Proc. IEEE Radio Wireless Symp., 2012, pp. 227–230.
[15] Wang Chunhua, Wan Quizhen, “A 0.18um CMOS Low noise amplifier using current reuse technique for 3.1 – 10.6 GHz UWB Receiver”, Journal of Semiconductors, Vol. 32, No. 8, Aug. 2011.
[16] A. Ismail, A.A. Abidi, “ A 3 -10 GHz low noise amplifier with wideband LC ladder matching network,” IEEE Journal of solid state circuits, Vol. 39, No. 12, pp. 2269 – 2277, Dec. 2004.
[17] A. I. A. Galal, R. K. Pokharel, H. Kanaya, and K. Yoshida, “1-5GHz Wideband Low Noise Amplifier using Active Inductor,” Proceedings of 2010 IEEE International Conference on Ultra-Wideband (ICUWB2010), 2010.

AUTHOR PROFILE

J.Manjula received her Bachelor degree in Electronics and Communication Engineering from Madras University in May 1996 and M. Tech. (VLSI Design) degree in Bharath University, Chennai in 2006. She is an Assistant Professor (Selection Grade) in the Department of Electronics and Communication Engineering at S.R.M. University, Kattankulathur, Chennai, India, since 2006.Presently, she is pursuing her Ph.D. degree in Electronics and Communication Engineering at S.R.M. University in the field of RF VLSI Design. Her research interests are design of analog circuits for RF systems, microwave integrated circuits and adaptive circuit designs. She is a life member of Advanced Computing Systems

Dr. S. Malarvizhi received her B.E. degree in ECE from Arulmigu Meenakshi Amman College of Engineering in 1989 and M.E from GCT, Coimbatore in 1990. She was awarded Ph.D degree from Anna University in 2006. Her research interests are wireless communications, sensor networks and FPGA implementation of communication algorithms. She has published more 100 papers in international journals and conferences and guided more than 10 Ph.D scholars.