ISSN (Print) : 2319-8613
ISSN (Online) : 0975-4024


# Design of Quantum circuit for Full Adder using HNG Gate

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***Abstract*— In the low power consumption, the reversible logic circuits are advantageous compared to the current ones, which is a good choice for the future design of computers. Among the characteristics of the reversible gates, the equality between the entries and the outputs, namely by the preservation of the parity of or circuits containing these gates have this same attribute. In this article we will base ourselves on a recent study of the FULL ADDER design to modify it and obtain improved results.**

**Keyword -** Quantum cost, number of garbage outputs, number of gates, delay, hardware complexity

## I. INTRODUCTION

The technology of integrated circuit manufacturing has undergone remarkable development in recent years [1]. According to the Landauer law [2], each lost bit generates a quantity of heat KTLn2, to avoid this dissipation we will use quantum computation [3] and reversible computation [4] that we use a gate the same type (reversible). In this article, we will modify the FULL ADDER circuit based on a recent study [5] while keeping the same functionality and improving the following characteristics Number of gates, Hardware complexity, Quantum Cost, Delay and Number of garbage outputs.HNG [4] is our key reversible gate that we will use based on a recent study to design a FULL ADDER improving the performance of this circuit.

## II. REVERSIBLE GATES AND THEIR PERFORMANCE CRITERIA

### *A. Reversible Gate*

In a reversible gate the number of inputs is equal to the number of outputs , in addition each input vector has a unique output vector, n is the number (of inputs and outputs) then our gate is named gate n * n reversible. Reversibility in computer mode means that no information is calculated at the state level. The fact that any previous step is done by doing an inverse calculation will be feasible, which is the object of the logical reversibility [4], which must be conjugated to the physical reversibility which prevents any kind of loss of energy in the form of heating. In the following, we will show some logical reversible gates concerned by this article.

### *B. Reversible gates used*

1) *New gate:* A reversible gate NG 3 * 3 Fig1[4], presented by its quantum implementation Fig2 [4], which shows us that its quantum cost is 11.


Fig. 1. New Gate

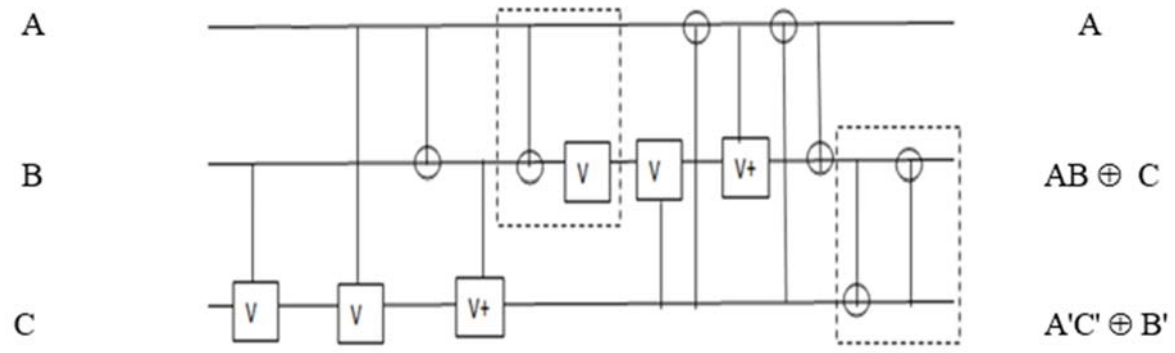


Fig. 2. Quantum Implementation of NG

In addition, the hardware complexity of NG gate is equal to: $2\alpha + 2\beta + 3\delta$ (α: number of CNOT gates β: number of ANDs δ : number of NOT gates).

*2) HNG gate: is* a reversible gate 4 * 4 Fig3[4] ,its quantum implementation is presented in Fig4 [4] which shows us that its quantum cost is 6.

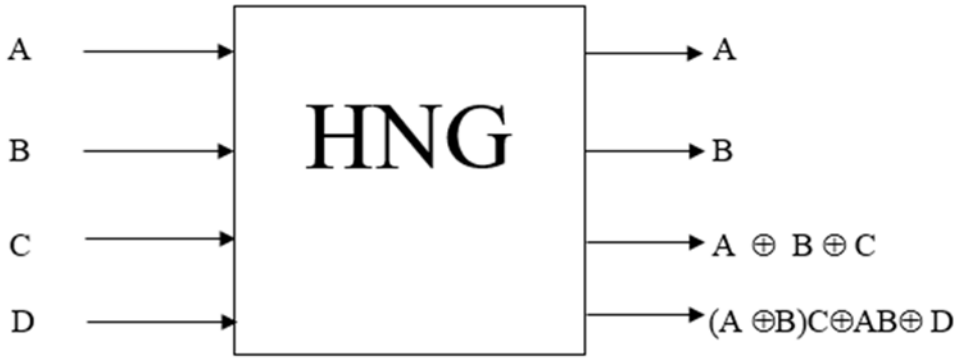


Fig. 3. HNG gate

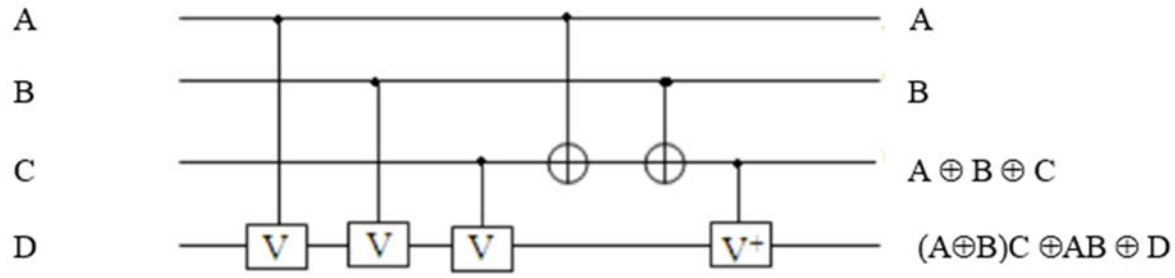


Fig. 4. Quantum Implementation of HNG

The hardware complexity of HNG gate is :$4\alpha + 2\beta$ (α: number of CNOT gates β: number of ANDs).

## III. Exploited Work

The FULL ADDER circuit is a circuit that combines both operations called SUM and CARRY whose equations are SUM= A ⊕ B ⊕ C and CARRY = (A ⊕ B)C ⊕ AB, shown in Fig 5 [5] with a classic model. Its reversible equivalent using NG gate is represented on figure 6, on which we are based Fig6 [5] to modify it while preserving the same functionality and improving its performances.

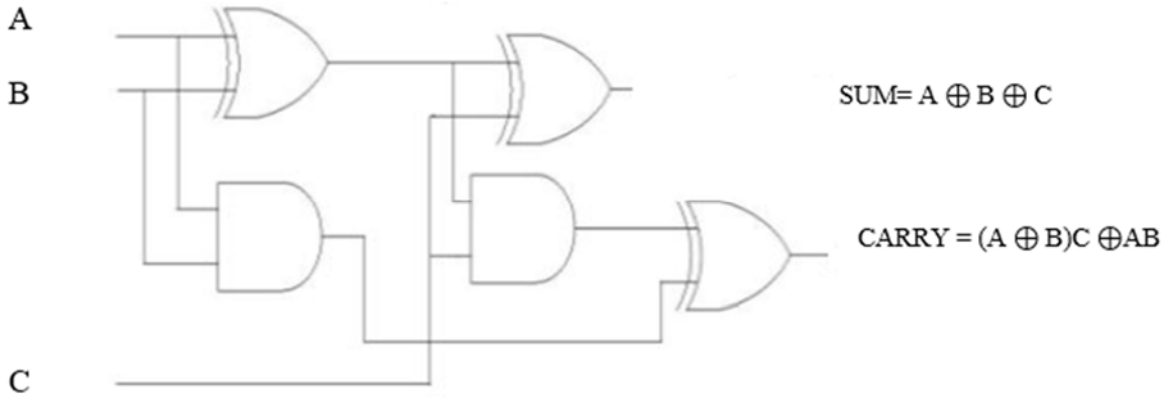


Fig. 5. Classical Full Adder Circuit

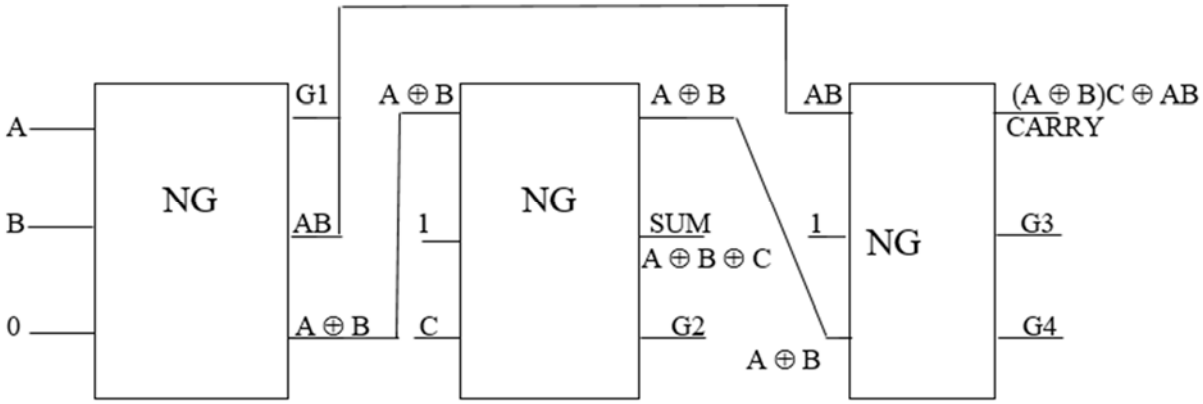


Fig. 6. Fault Tolerant Proposed Full Adder Circuit Using NG

So to get the same outputs of this circuit and keeping the same functionality we just put the input D to 0 (D = 0) in HNG Gate Fig7.

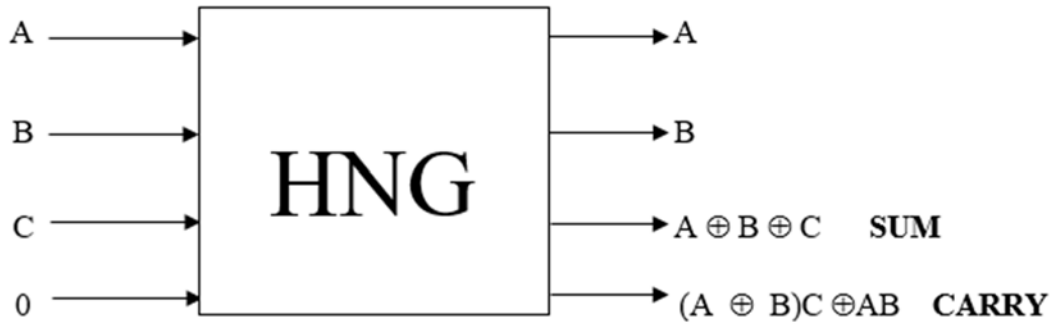


Fig. 7. Our design of Full Adder Circuit

By making a comparison between our proposed circuit and the exploited circuit, we obtain the result mentioned in the following table:

TABLE1: the results obtained from the design of FULL ADDER circuit using HNG

| | **Number of Gates** | **Quantum Cost** | **Hardware Complexity** | **Number of garbage outputs** | **Delay** |
|---|---|---|---|---|---|
| Our design | 1 | 6 | $4\alpha + 2\beta$ | 2 | 1 |
| Exploited study [5] | 3 | 33 | $6\alpha + 6\beta + 6\delta$ | 4 | 3 |

From these results we deduce that we have minimized compared to the model exploited:

- 2gates
- the quantum cost of 81,81%
- Delay of 2 units
- 2 of outputs garbage
- Hardware complexity at 33,33% of CNOT gates, 66,67% of AND gates and eliminating all gates of NOT.

## IV. CONCLUSION

The reversible logic makes it possible to minimize the energy consumed of all the information lost in a circuit. This article exploited an old FULL ADDER circuit to design a new one by using logical inversion gates while seeking to improve performance criteria by minimizing: the number of gates, the waste outputs, the quantum cost, the hardware complexity and delays, which outperforms the article we based on [5].

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[5] International Journal of Application or Innovation in Engineering Management (IJAIEM) Web Site: www.ijaiem.org Email: editor@ijaiem.org Volume 6, Issue 6, June 2017 ISSN 2319 - 4847 Synthesis of Quantum Circuit for FULL ADDER Using KHAN Gate Madhumita Mazumder West Bengal University of Technology, West Bengal