# Reversible Design Of Asynchronous Sequential Circuits

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***Abstract*—Reversible logic is becoming increasingly important in the design of low-power CMOS circuits, reversible circuits have given rise to what is called a quantum computer which is introduced by them with the aim of minimizing energy losses in the form of heat at the end of the lost bits and of performing more complex functions by taking into account certain criteria showing their performance, namely a number of gates ,a number of outputs garbage, a quantum cost, a delay and a hardware complexity. in this article, we will try to exploit a pre-existing article designing the asynchronous circuits in reversible mode, namely Circuit Implementation by latch using reversible logic gates and T Flip Flop sensitive to falling edge clock using reversible logic gates in order to obtain better results, by increasing their following performances quantum cost and the hardware complexity compared to our basic article.**

**Keyword -** asynchronous sequential circuits , hardware complexity, quantum cost

## I. INTRODUCTION

The technology of integrated circuit manufacturing has undergone remarkable development in recent years [1]. According to the Landauer law [2], each lost bit generates a quantity of heat KTLn2, to avoid this dissipation we will use quantum computation [3] and reversible computation [4] that we use a gate the same type (reversible). In this article, the design of circuit implementation by latch using reversible logic gates and Flip Flop sensitive to falling edge clock using reversible logic gates ,while keeping the same functionality and improving the following characteristics Hardware complexity , Quantum Cost .PG [9] is our key reversible gate that we will use based on a recent study [10] to design and improving the performance of this circuit.In the irreversible circuit each lost bit generates a loss of heat described by KTln2 joules of or K: Constant of BOLTZMAN T: Absolute temperature related to the computation, Formula established by Landauer [1]. In the reversible case Bennett showed that this said amount of heat would not occur [2], the proof is that this quantity of heat is related to the number of bits lost in an irreversible circuit, In the case of the ambient temperature this so-called quantity of heat for a lost bit is 2:9 10 21J[3]. In addition, this dissipation adversely affects the performance and life of the circuits, and to ensure minimal energy consumption and heat loss, new circuit technology has been triggered. [4]. These circuits have a bijection between its inputs and outputs so a reversible gate NXN can be represented by :

$$Iv = (I1, I2, I3, I4, \ldots\ldots IN) Ov = (O1, O2, O3, O4, \ldots\ldots ON)$$

Where $Iv$ and $Ov$ unveil the input and output vectors respectively. In the irreversible gates one can not deduce the input vector in a unique way from the output one [5].While in a reversible circuit each input vector is associated with a single output vector and vice versa. Each reversible gate having k inputs must have k outputs and will be named k * k reversible gate. The asynchronous circuits used a local exchange between the modules in case of need instead of using a global clock for synchronization. in this article we will be based on a recent study [10] for the design of circuit implementation by latch using reversible logic gates and Flip Flop sensitive to falling edge clock using reversible logic gates which we will modify to obtain better results Their design is becoming increasingly important as it helps to minimize energy consumption, improve performance and robustness [6]. That will be explained in detail later in this paper.

## II. REVERSIBLE QUANTUM GATES AND CIRCUITS

A reversible gate associated for each entry one and only exit. Digits or bits are concerned with reversible gate (or conventional reversible gates). They are exploited in certain techniques and technologies namely CMOS Optics nanotechnology the qubits are concerned by the quantum gates being the subject of quantum information unit. This information is demonstrated by a state vector in a two-level quantum mechanics system that is formally equivalent to a two-dimensional vector space on complex numbers [7]. In the memory of a conventional discrete computer its units are in the form of bits, two valued conventional variables. By similarity, a qubit, will be represented by a two-level quantum system. In case the eigenstates of the quantum variable are generated by | 0 > and | 1 >. This brings us back to the discrete states of a classical bit, 0 and 1 [8]. There are various reversible gates. In the following we will show the ones that are concerned by this paper by revealing their performances [9] .showing the structure of each gate Reversible Gate, Name of the Structure, Quantum implementation , Quantum cost , and Hardware complexity.

### *A. Feyman Gate*

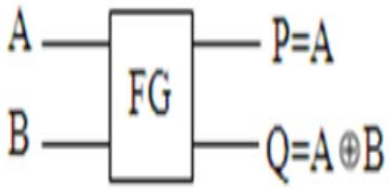


Fig 1 Feyman Gate

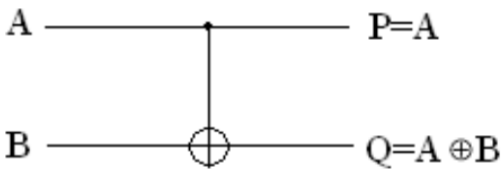


Fig2: Quantum implementation of Feyman Gate

QC=1 $T = 1\alpha$(α: number of CNOT gates β:number of ANDs δ: number of NOT gates).

### *B. Fredkin Gate*

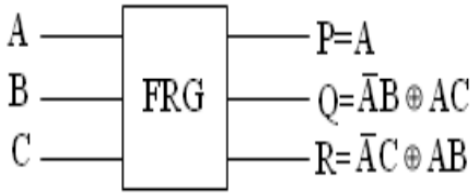


Fig3: Fredkin Gate

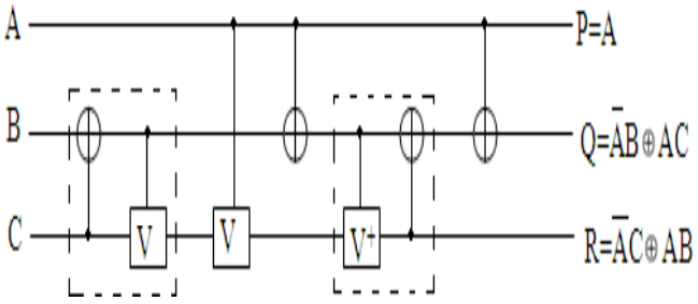


Fig4: Quantum implementation of Fredkin Gate

QC=5 $T = 2\alpha + 4\beta + 1\delta$(α: number of CNOT gates β:number of ANDs δ: number of NOT gates).

*C. New Gate*

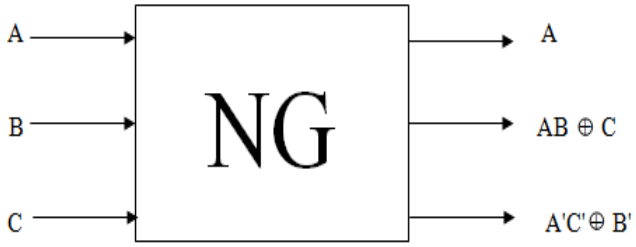


Fig5: New Gate

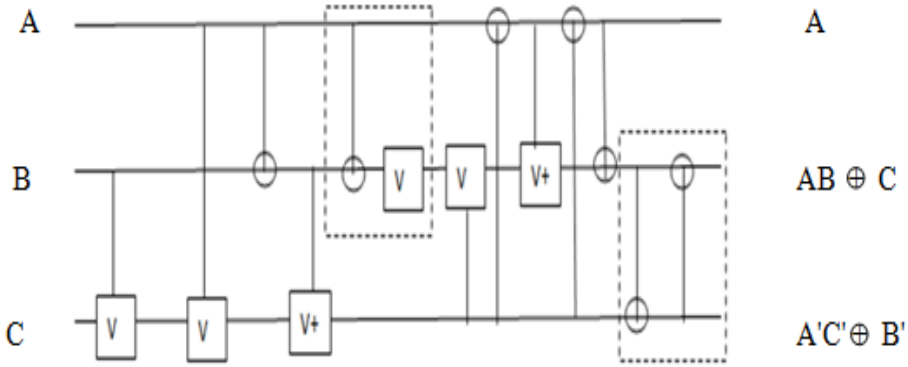


Fig 6: Quantum implementation of New Gate

QC=11 $T = 2\alpha + 2\beta + 3\delta$(α: number of CNOT gates β:number of ANDs δ: number of NOT gates).

*D. Peres Gate or New Toffoli gate*

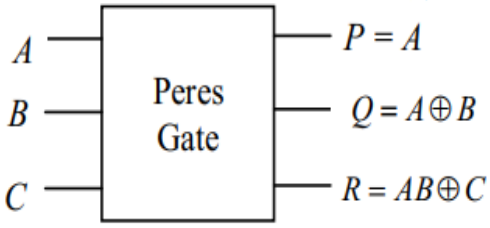


Fig 7: Peres Gate

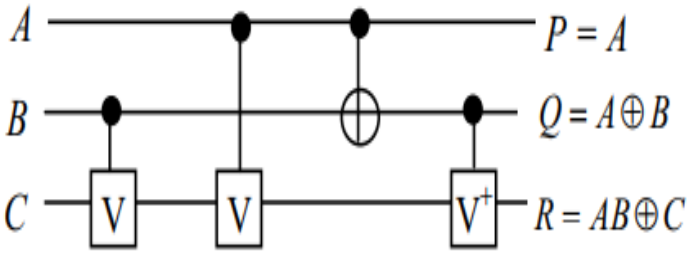


Fig 8: Quantum implementation of Peres Gate

QC=4 $T = 2\alpha + \beta$ (α: number of CNOT gates β:number of ANDs δ: number of NOT gates).

## III. EXPLOITED WORK

We base ourselves on certain recent circuits, [10] ,Circuit Implementation by latch using reversible logic gates and Flip Flop sensitive to falling edge clock using reversible logic gates to modify them and have better results, in terms of: hardware complexity and quantum cost, starting with:

*A. CIRCUIT IMPLEMENTATION BY LATCH USING REVERSIBLE LOGIC GATES*

Then we will propose The Circuit Implementation by latch using reversible logic gates. fig10 based on a recent circuit fig9 [10] trying this time to modify it by minimizing the quantum cost and hardware complexity.

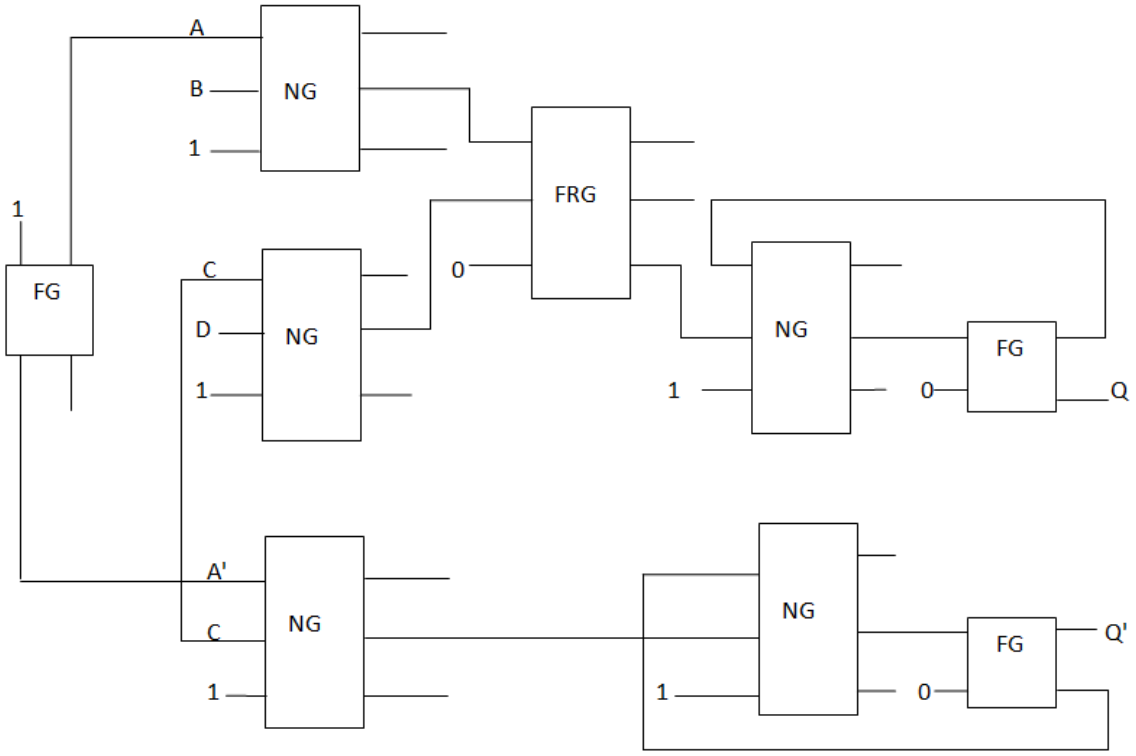


Fig 9: The Circuit Implementation by latch using reversible logic gates

After replacing New gate and Fredkin Gate by Peres Gate we will get our new design we draw our results obtained in Table1 After replacing New gate and Fredkin Gate by Peres Gate we will get our new design In the following table we will show our results Table 1

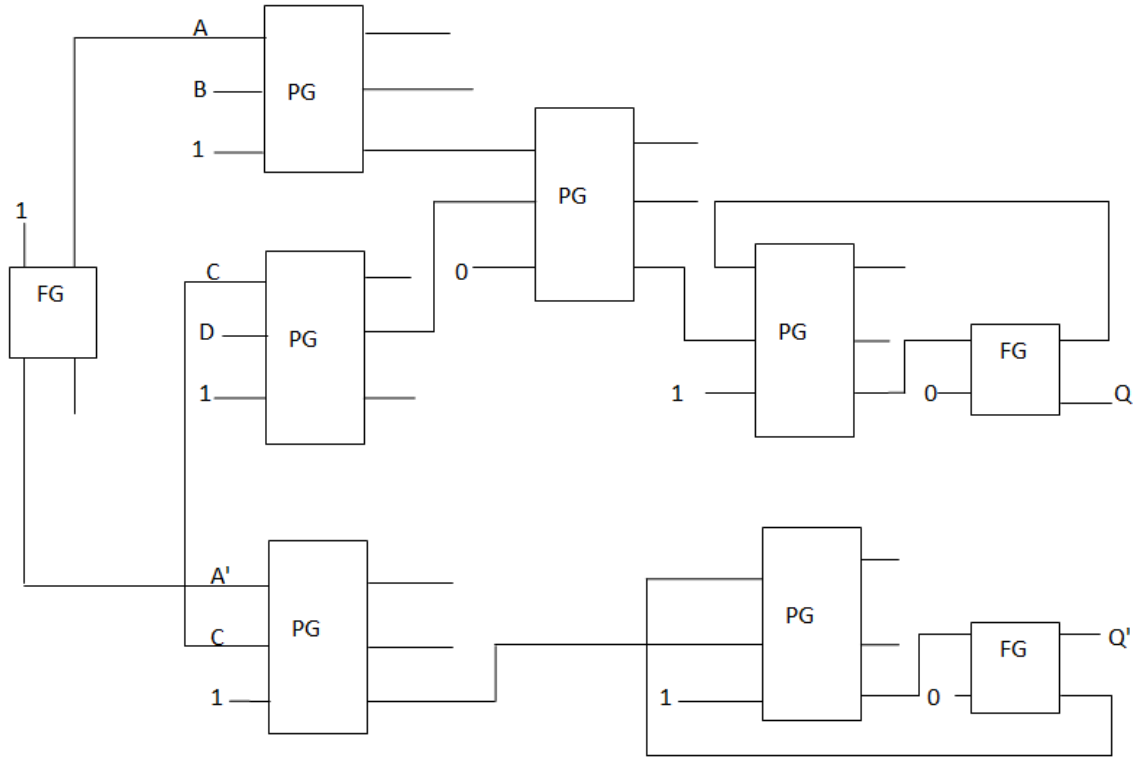


Fig 10: The Circuit Implementation by latch using reversible logic gates our design

In the following table we will show our results Table 1

Table 1 Evaluation of Circuit Implementation by latch using reversible logic gates our design

| Locking Circuit Design Using Reversible Logic Gates | Quantum Cost | Hardware Compelxity |
|---|---|---|
| **Our design** | 27 | $15\alpha + 6\beta$ |
| **Exploited study [10]** | 63 | $15\,\alpha + 14\,\beta + 16\,\delta$ |

We notice that we have decreased:

-the quantum cost of **57.14%**

-Hardware complexity, at **57.14%** of AND gates by eliminating all NOT gates compared to the model used.

*B. T FLIP FLOP SENSITIVE TO FALLING EDGE CLOCK USING REVERSIBLE LOGIC GATES*

After we will propose T Flip Flop sensitive to falling edge clock using reversible logic gates Fig12 based on a recent circuit Fig11 [10] minimizing quantum cost and hardware complexity.

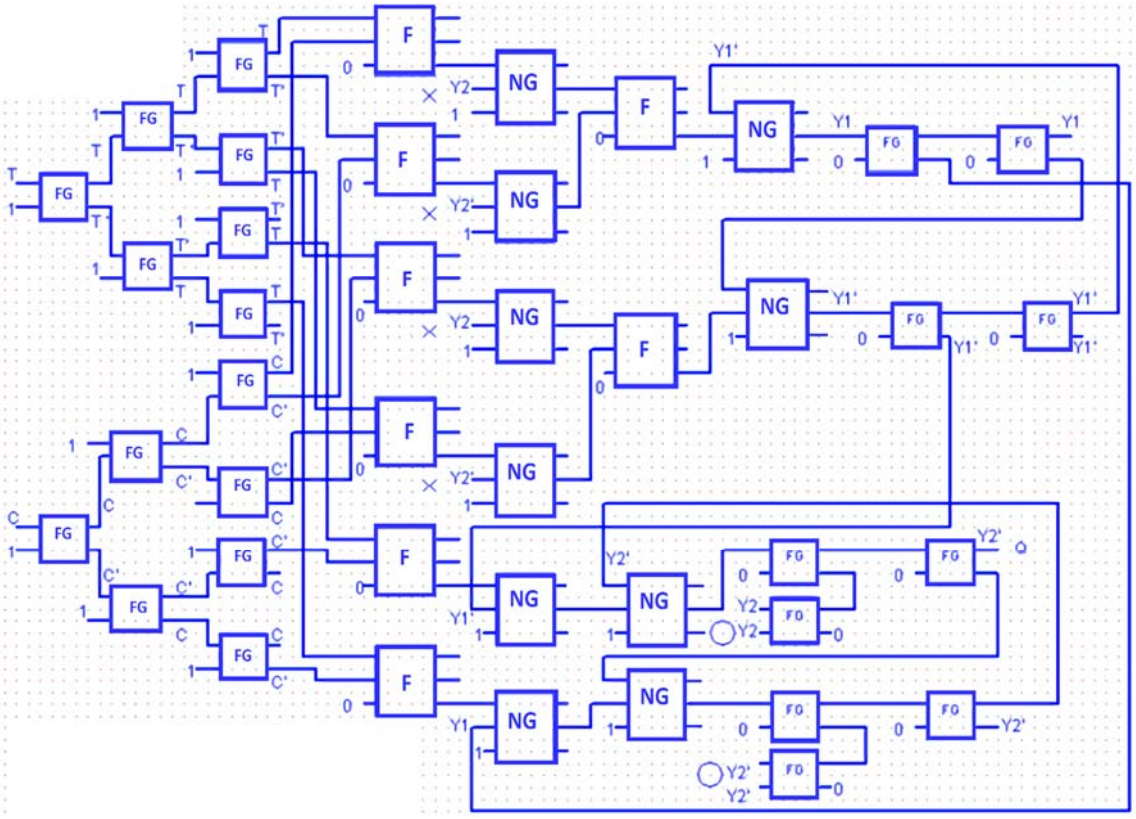


Fig 11: T Flip Flop sensitive to falling edge clock using reversible logic gates

Then replacing all FRG and NG gates by PG we will get our ne new design Fig 17, we draw our results obtained in Table 2 that assesses the performance of our work. Fig 9 shows design of this circuit in reversible mode based on an old study.

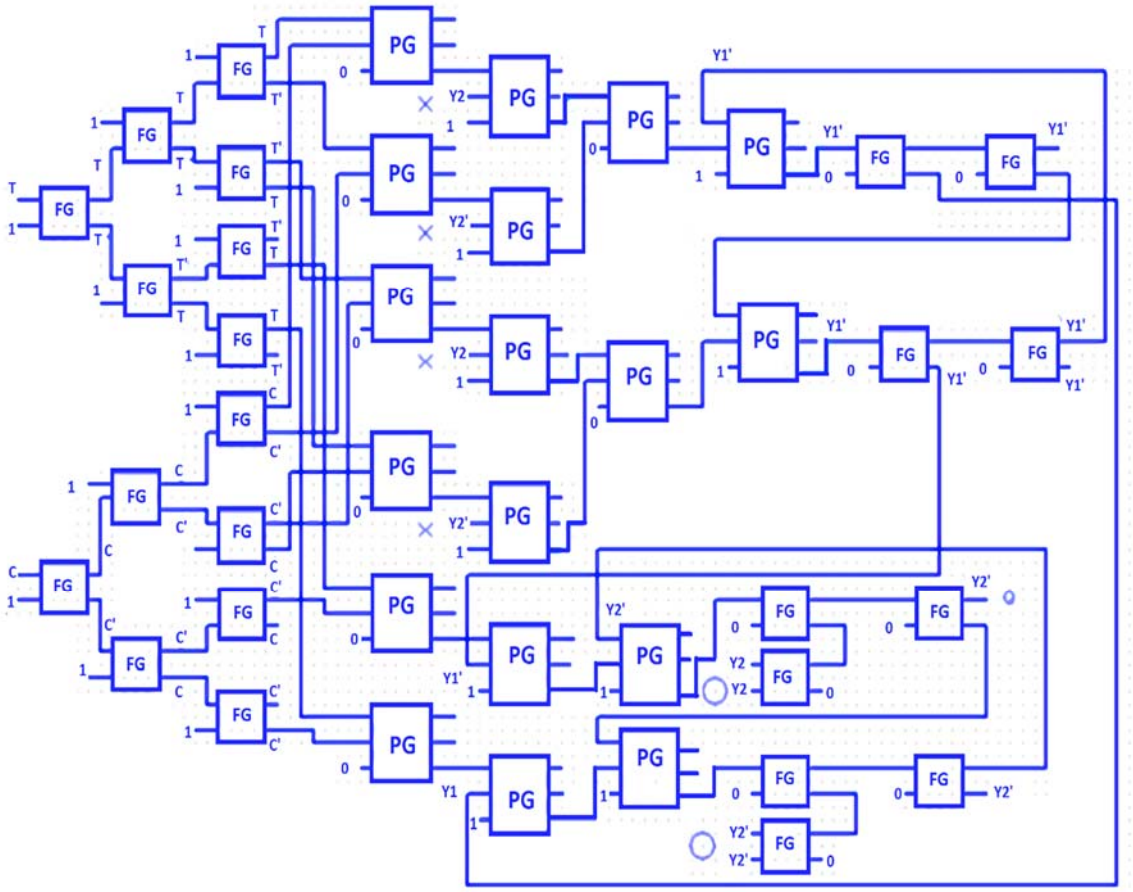


Fig 12: T Flip Flop sensitive to falling edge clock using reversible logic gates Our design

In the following table we will show our results Table 2

Table 2 Evaluation of Circuit T Flip Flop sensitive to falling edge clock using reversible logic gates Our design

| Flip Flop sensitive to falling edge clock using reversible logic gates | Quantum Cost | Hardware Complexity |
|---|---|---|
| **Our design** | 96 | $60\alpha + 18\beta$ |
| **Exploited study [10]** | 174 | $60\alpha + 52\beta + 38\delta$ |

We notice that we have decreased:

-the quantum cost of **44.82%**

-Hardware complexity **65,38 %** of AND gates by eliminating all NOT gates compared to the model used

## IV. CONCLUSION

The reversible logic contributes to, minimize the energy consumed in a circuit and all lost information. This article has exploited ancient ones to design asynchronous circuits by using logical reversing gates while trying to improve performance by minimizing: the quantum cost, hardware complexity from which we obtained better and more remarkable results compared to the previous research. Waiting for more new reversible gate to be found thus we can improve and get more outperforming circuit.

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[10] Bahram Dehghan / International Journal of Engineering and Technology (IJET) Design of Asynchronous Sequential Circuits using Reversible Logic Gates Bahram Dehghan Islamic Azad University, Sarvestan Branch, Department of Electrical Engineering, Sarvestan, Iran Bahramdehghan1@gmail.com