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Design and FPGA Implementation of Intelligent Helmet Hardware Chip for Safe Drive

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***Abstract*— The research article is based on a very serious issue of number of deaths of two wheeler drivers in India due to severe head injuries occurred because of not wearing helmets. Statistics data of India shows in year 2015 total 1,44,391 accidents took place with two wheelers and 36,803 deaths occurred and out of which 19.6 % were due to head on collision and most of them due to not wearing helmet. The Flex sensor based a novel system is developed to address this issue, which is designed in such way that vehicle will not be ignited unless person wears a helmet which assures the safety of driver. The paper focuses on the chip design and implementation of hardware system on FPGA for helmet. The high speed controller is designed with the help of VHDL programming language in Xilinx 14.2 ISE software and synthesized on Virtex-5 FPGA. The function simulation is also carried to test the different test cases with Modelsim 10.1b. The developed system supports the frequency of 781.250 MHz, which can be an optimal solution for the intelligent helmet.**

Keyword - Helmet, Safety, two- wheeler, controller, FPGA

I. INTRODUCTION

Buckley, Lisa, et al.[1] shows statistical data for motor cycle crash in Michigan during year 2012-2014. Study on helmet use and its characteristics was carried out. The aim was to increase helmet use for the motorcyclists because avoiding it results in serious fatal and non-fatal injuries. Winn, Gary L. et al [2] discusses about bicycle safety module to encourage people for wearing helmet by demonstrating the knowledge with the help of students. It was observed that during BSM helmet usage improves upto 100% but fell down after it was over. It has been concluded that a periodic orientation programs are required to encourage the people for safety issues. Richmond, Sarah A., et al. [3] discusses about bicycle skill training program for young people of age less than 19 years. The target was to study the effect on bicycle related injuries after training. The study shows eight of 16 reported the significance gain in knowledge that results in improvement in skills after training program. Houten, Ron et al [4] shows a study on education on wearing helmet and importantly wearing it correctly. Study has been taken on three middle schools. A study on the behavior of children inside the school and away from close proximity of the school has been studied. The study shows different behavior of children during morning and afternoon time. Kelly, Patrick, et al. [5] discusses a study on the impact of helmet usage on motorcycle crash. A study has been done and it was concluded that helmets are helpful in reducing the impact of head injuries during motorcycle crash and reduces the cost of health issues than non-helmeted people. Muelleman, Robert L. et al [6] shows the study of number of serious head injuries in Nebraska and Midwestern states with helmeted and unhelmeted motorcyclists. The study shows serious head injury with helmeted motorcyclists were 5% lower than unhelmeted. Shankar, Venkataraman et al [7] addresses issues related to variables considered for analysis of motorcycle crushes and concerns about prior research contents. It focuses on five levels which needs to be considered along with helmet use. Xu Xiang Rong [8] talks about wireless communication with mobile phone or other Bluetooth devices with helmet having inbuilt Bluetooth device. Prabhakaran, N. et al [9] discusses an automatic wiper system during precipitation, which reduces the number of accidents due to distraction of driver for manual adjustment of wipers. Gehlot, Anita et al. [10] describes a WPAN and LabVIEW based system for monitoring the water quality at home through RF modem. The designed system is capable of giving the early warning for the contaminated water.

II. SYSTEM DESCRIPTION

An intelligent helmet is designed with flex sensor which assures not to ignite the vehicle unless driver wears the helmet. The whole system comprises of two segments- Helmet node and two wheeler node. The helmet node as shown in fig.-1 comprises of four flex sensors, controller and RF modem. The Flex sensors gives a cumulative data to controller when helmet is wear by the driver and sends this data to two wheeler node through RF modem. The two wheeler node which comprises of controller and RF modem compares the received value from helmet to already stored threshold value to controller. If the data received from helmet is more with the predefined value at two wheeler node then only vehicle will be ignited through a relay.

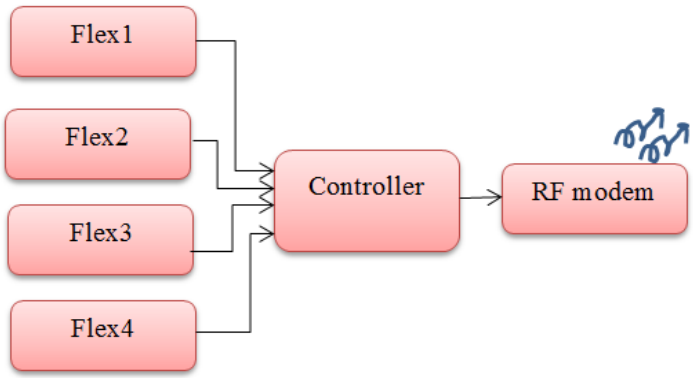

Fig.- 1 Block diagram of helmet node

This paper focuses only towards the controller design for the helmet node. The paper focuses on the chip design and implementation of hardware system on FPGA.

The controller is designed for four analog inputs from flex sensor. As flex sensors gives analog output and controller only understands the digital values so to process the signal analog to digital converter is also placed with the sensor inputs to the controller. The average value of four inputs are taken. This value is then displayed on LCD to verify the data when actual hardware implementation is done. The same value is transmitted to two wheeler node wirelessly through RF modem. The RF modem is a device which is capable of transmitting the data within the range of 30 meters or more depending on the frequency of RF modem used. The range of 30 meters can be achieved with a modem of 433 MHz of frequency. The RF modem is superior to IR modem as it doesn't need line of sight for operation.

III. Results and Discussion

The controller is designed with the help of VHDL programming language in Xilinx 14.2 ISE software and then synthesized on Virtex-5 FPGA. The Modelsim 10.1b simulation is done to test the different test cases.

The RTL view transmitter section of the intelligent helmet system is shown in fig.2. It depicts all the possible inputs and outputs of the design and internal architecture is shown in fig.3. The detail of the pins is discussed in Table 1.

Fig. 2 RTL view of helmet node controller

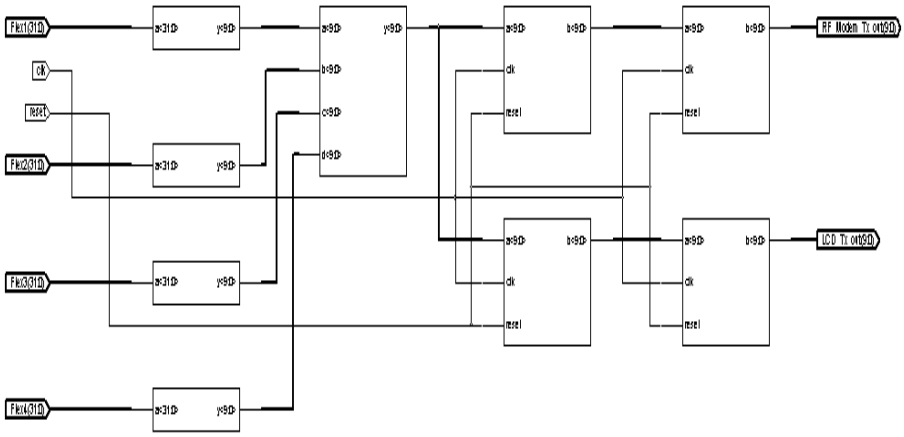

Fig. 3 Internal architecture of the controller of helmet node

TABLE I. Pin description of controller of helmet node

Pin	**Function**
Flex1<31:0>	It is the input of the flex sensor 1
Flex2<31:0>	It is the input of the flex sensor 2
Flex3<31:0>	It is the input of the flex sensor 3
Flex4<31:0>	It is the input of the flex sensor 4
Selection_logic<1:0>	Input selection logic to get the input data with respect to flex1, flex 2, flex 3, flex 4
Clk	Input to give the clock signal at the helmet node
Reset	Input to give the reset signal in synchronization to clock input signal
LCD_out<9:0>	The average values of flex1, flex 2, flex 3 and flex 4 is displayed on the 10 bit LCD out at helmet node (Output)
RF_Modem_Tx_out<9:0>	The Transmitted outputs displayed correspond to LCD section in transmitter side.

The modelsim wave output of the helmet node is shown in fig.4(a) and fig.4(b). The fig.4(a) presents the output for 1 test case. The fig.4(b) presents the output for 5 test cases. In the waveform flex1, flex 2, flex 3and flex4 presents the flex sensor inputs. The clk and reset are the default inputs. The selection of sensor values is done based on slection_logic[1:0]. The output of flex 1, flex 2, flex 3 and flex 4 first converted to digital using 10 bits ADC shown in fig.3 ADC1[9 : 0], ADC2 [9 : 0], ADC3 [9 : 0] and ADC4 [9 : 0] corresponding to flex1, flex2, flex 3 and flex4, USART_ in shows the value of USART transmission. In the same way lcd_tx_in [9:0] and lcd_tx_out [9:0] shows LCD input and output. Rf_modem_tx_in [9:0] and Rf_modem_tx_out [9:0] present the input and output of the RF modem input and output.

The simulation waveforms are tested for following values.

Case 1: flex1 = 100 , flex 2 =200 , flex 3 = 300 and flex 4 = 0 and corresponding output is Rf_modem_tx_out [9:0] = 0011001000 in binary and 200 in decimal.

Case 2: flex1 = 200 , flex 2 =300 , flex 3 = 400 and flex 4 = 0 and corresponding output is Rf_modem_tx_out [9:0] = 0100101100 in binary and 300 in decimal.

Case 3: flex1 = 300 , flex 2 =400 , flex 3 = 500 and flex4 = 0 and corresponding output is Rf_modem_tx_out [9:0] = 0110010000 in binary and 400 in decimal.

Case 4: flex1 = 400 , flex 2 =500 , flex 3 = 600 and flex4 = 0 and corresponding output is Rf_modem_tx_out [9:0] = 0111110100 in binary and 500 in decimal.

Case 5: flex1 = 500 , flex 2 =600 , flex 3 = 700 and flex4 = 0 and corresponding output is Rf_modem_tx_out [9:0] = 1001011000 in binary and 600 in decimal.

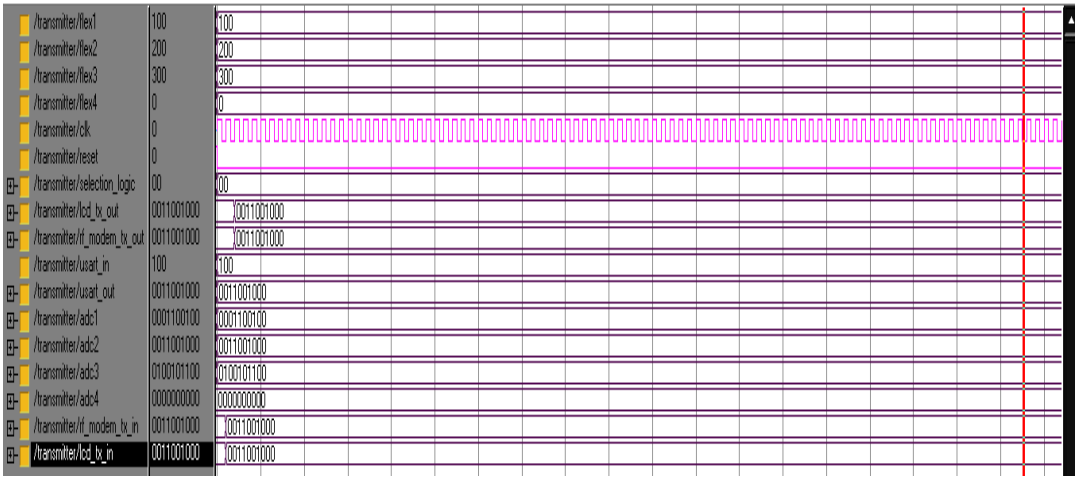

Fig. 4(a) Modelsim waveform for test case-1

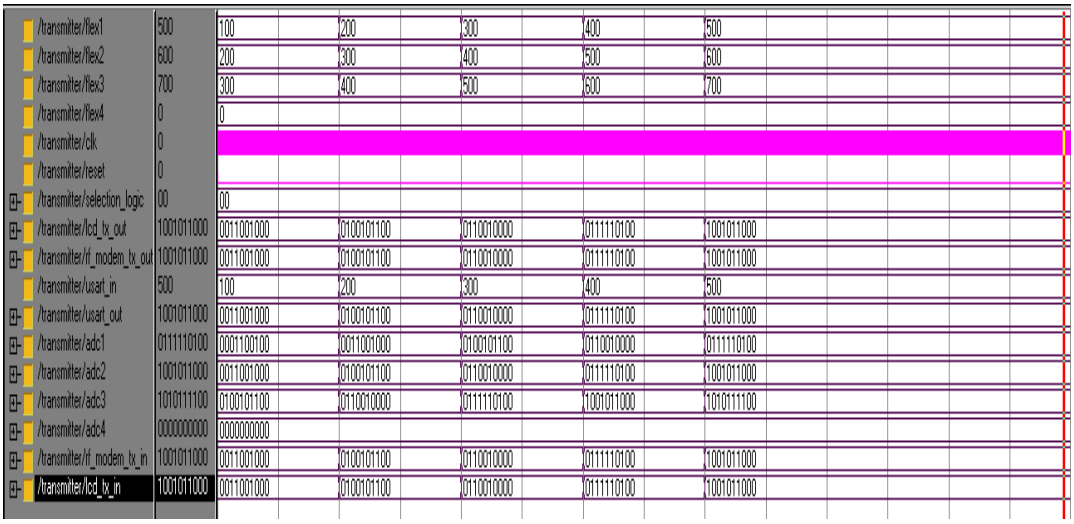

Fig. 4(b) Modelsim waveform for all test cases

FPGA Synthesis Report of helmet node

The design is synthesized on Spartan-6 FPGA. The target device is Xc6slx-45-2csg324. The hardware summary report shows the utilization of LUTs, Flip flops, inputs and output, value of slice registers and buffers and CPU memory etc. Table-2 shows the hardware summary report of helmet node. The timing values shows the value of minimum and maximum clock timing and frequency support.

Timing Summary

Speed Grade: 2

Period value minimum: 1.280ns

Frequency value as maximum: 781.250MHz

Arrival time value before clock as minimum: 24.084ns

output time required after clock as maximum: 4.162ns

CPU memory usage is 251564 kilobytes

TABLE II. Hardware Summary report of helmet node

Transmitter Project Status			
Project File:	ADC.xise	**Parser Errors:**	No Errors
Module Name:	Transmitter	**Implementation State:**	Synthesized
Target Device:	xc6slx45-2csg324	**• Errors:**	No Errors

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	20	54576	0%
Number of Slice LUTs	779	27288	2%
Number of fully used LUT-FF pairs	0	799	0%
Number of bonded IOBs	118	218	54%
Number of BUFG/BUFGCTRLs	1	16	6%

IV. CONCLUSION

The controller for proposed system is designed with hardware description language environment and results are analyzed with Virtex-5. The controller is developed with four analog inputs from flex sensor and two outputs for serial LCD and RF modem. The LCD is connected only to display the cumulative result from flex sensors. The simulation results shows that the designed controller is working on 781.250 MHz which is very high if it is compared with existing controllers for example AVR Atmega-16 works on max. frequency of 16 MHz which shows high speed of designed system. The minimum period value is calculated as 1.280ns, arrival time is 24.084ns and the CPU memory usage is 251564 kilobytes. The designed chip can be a boon to VLSI industries as an optimal solution to the proposed system.

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